

HDL Implementation of Vending Machine Controller

*The objective here is to design Vending Machine Controller which accepts money inputs(*i* and *j*) in any sequence and delivers the products when the required amount has been deposited and gives back the change. The problem is explained with ASM chart in section 11.6 of the book *Digital Principles and Applications* by Leach, Malvino and Saha, TMH, 2006. Here an additional facility is provided to the user. It is possible to withdraw the deposited money in between if the customer wishes so by pressing a push button. Refer to simple full adder design and implementation given in this OLC.*

SPECIFICATIONS:

1. Price of the product=Rs.3.
2. Possible money inputs=Rs.2 and Re.1.
3. Product to be delivered when Rs.3 or Rs.4 is reached.
4. A Push button is there (pu) which indicates the cancellation of transaction and the return of the amount deposited.

VERILOG CODE:

```
/*  
Here  
i=0 indicates no coin has been detected.  
i=1 and j=0 indicates the detection of Re.1 coin.  
i=1 and j=1 indicates the detection of Rs.2 coin.  
pu indicates push button to cancel the transaction.  
Output p and c indicates the product delivery and coin return respectively.  
*/  
module vend(pu,i,j,rst,clk,p,c);  
input pu,i,j,rst,clk;  
output p,c;  
reg [2:0] state,NS;  

```

```

S4:NS=S0;
S5:NS=S0;
S6:NS=S5;
S7:NS=S0;
endcase

```

```

assign
{p,c}={(state[0]&state[1]&~state[2])|(~state[0]&~state[1]&state[2]),(state[2]&~state[1])|
(state[2]&~state[0])};
endmodule

```

CODE STIMULATION:

The above code is stimulated by writing a test bench. A specific case of a test bench is shown below.

```

module testbench();
reg pu,i,j,rst,clk;
wire p,c;
vend test(pu,i,j,rst,clk,p,c);

```

```

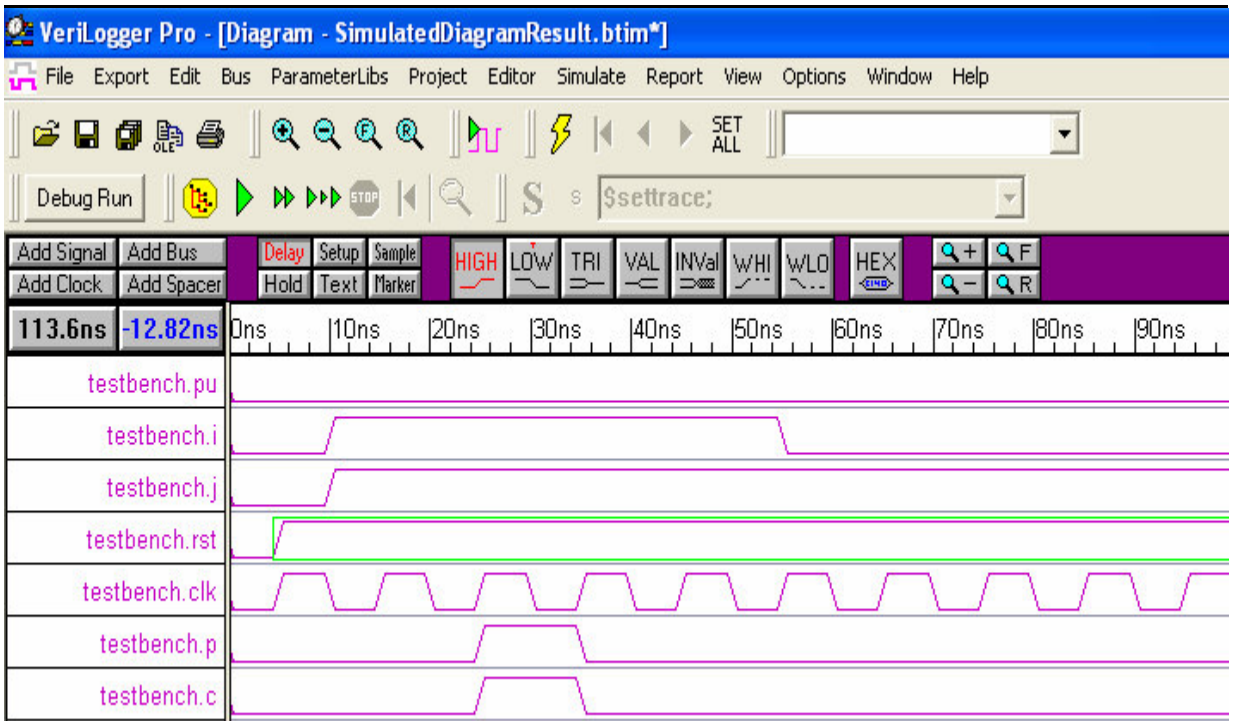
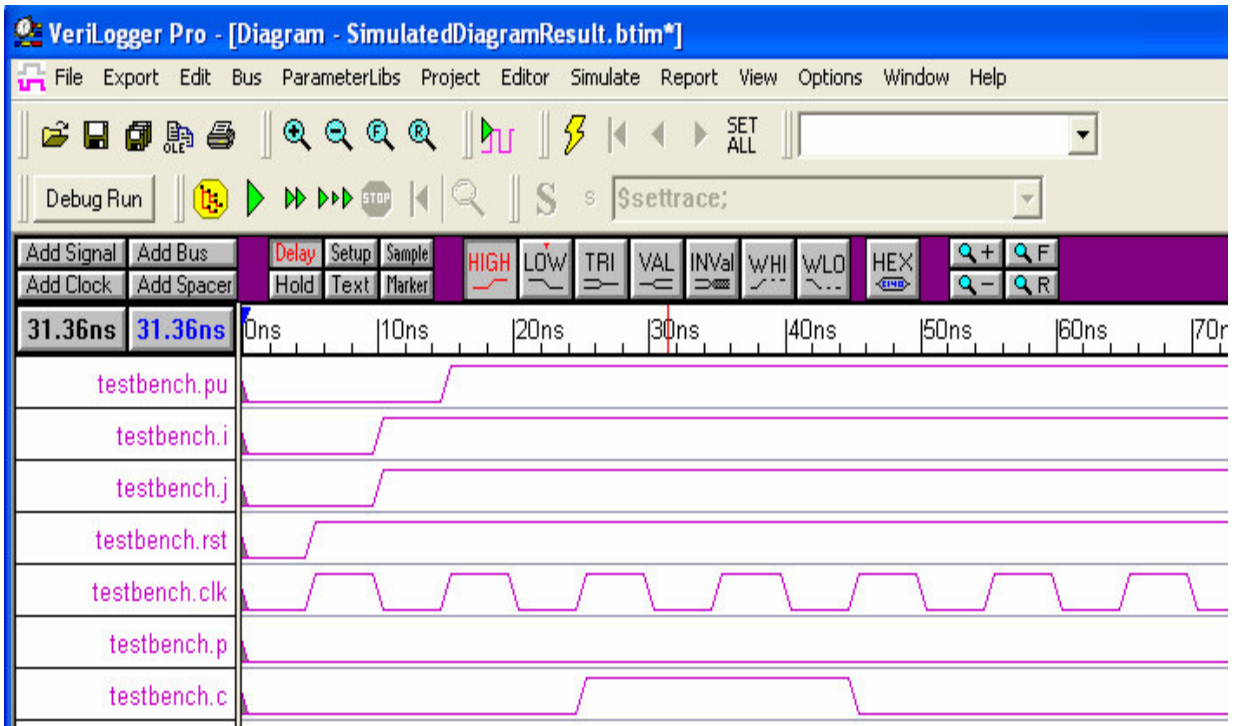
always
#5 clk=~clk;
initial
begin
i=1'b0;
j=1'b0;
clk=1'b0;
rst=1'b0;
pu=1'b0;
#5 rst=1'b1;
#5 i=1'b1;
#5 pu=1'b1;
#100 $finish;
end
endmodule

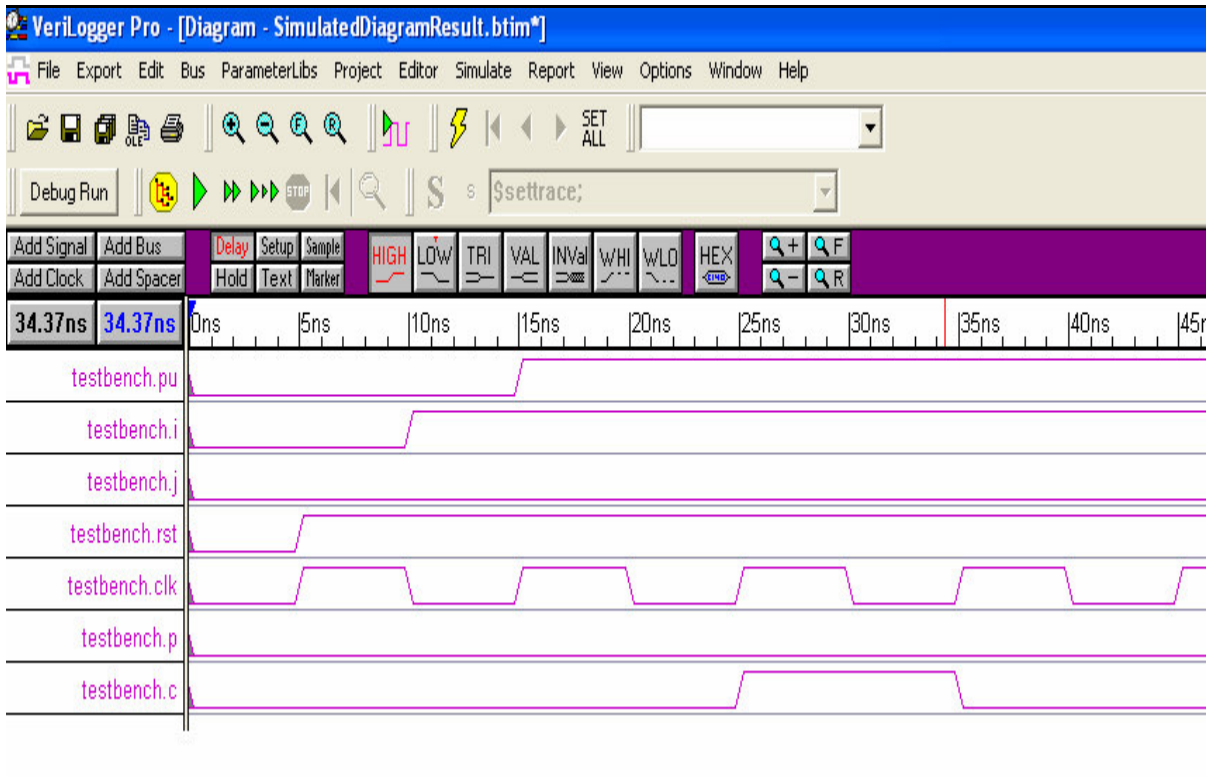
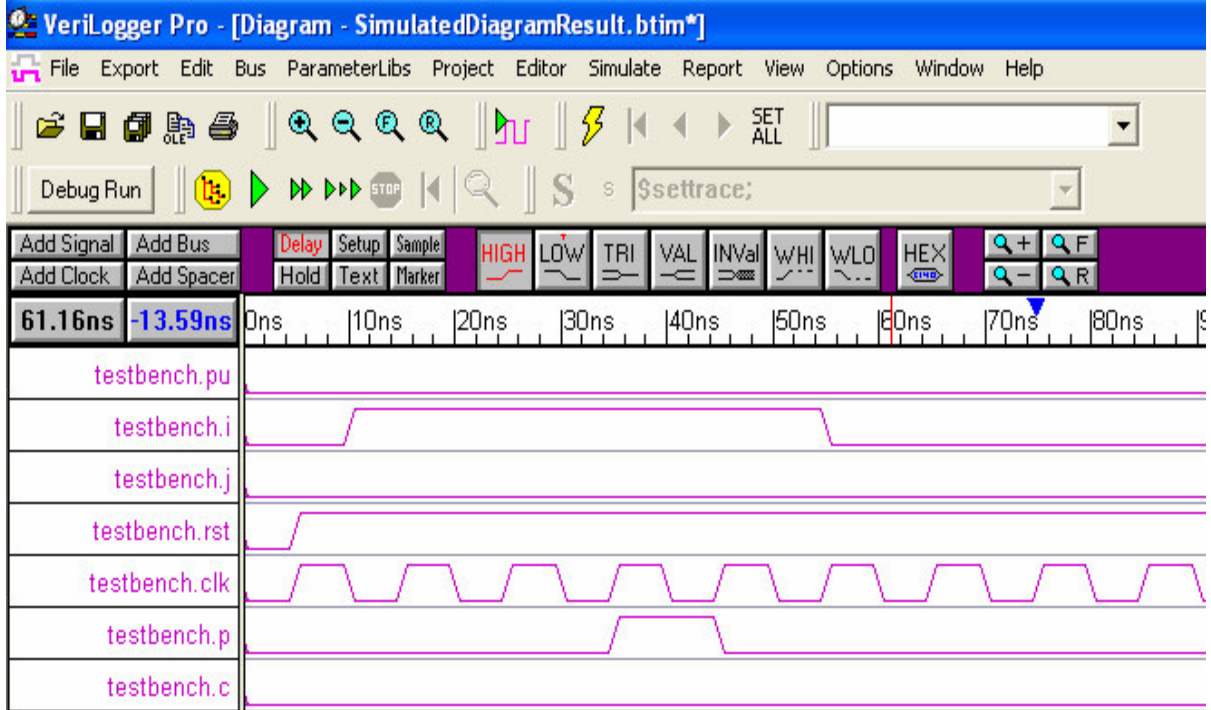
```

I/O WAVEFORMS:

The 4 Screenshots below show

1. Return of Rs.2 after push button is pressed
2. Delivery of product and return of Re.1 after Rs.4 is received.
3. Delivery of product after Rs.3 is received.
4. Return of Rs.1 after push button is pressed





SYNTHESISED CIRCUITS:

RTL SCHEMATIC

The screenshot displays the Xilinx Project Navigator interface. The main window shows an RTL schematic with two multi-bit input blocks on the left connected to a central multi-bit output block. A net labeled "Net = _n0007" is shown connecting the two output blocks. The left sidebar contains an "Instance Contents" panel with expandable sections for Pins, Nets, and Instances. Below this is a "Select the Modules or Snapshot tab" panel with the text "(No Processes Available)". The bottom console window displays the following synthesis results:

```
Minimum period: 6.351ns (Maximum Frequency: 157.456MHz)
Minimum input arrival time before clock: 7.866ns
Maximum output required time after clock: 10.502ns
Maximum combinational path delay: No path found
.....
```

The Windows taskbar at the bottom shows the Start button and several open applications: Xilinx - Project Naviga..., Adobe Acrobat Profe..., VeriLogger Pro - [Dia..., and architecturalviewofm... The system clock indicates 6:41 PM on 10/81/974.

One of the blocks of RTL schematic

The screenshot displays the Xilinx Project Navigator interface. The main window shows an RTL schematic with two multi-bit registers connected to a central bus. The bus is labeled "Net = _n0007". The left sidebar contains the "Instance Contents" panel, which is currently empty. Below it, the "Select the Modules or Snapshot tab" panel shows "(No Processes Available)". The bottom status bar indicates the current design is "vend.ngr".

The console window at the bottom displays the following timing analysis results:

```
Minimum period: 6.351ns (Maximum Frequency: 157.456MHz)
Minimum input arrival time before clock: 7.866ns
Maximum output required time after clock: 10.502ns
Maximum combinational path delay: No path found
```

The Windows taskbar at the bottom shows the Start button and several open applications: Xilinx - Project Naviga..., Adobe Acrobat Profe..., VeriLogger Pro - [Dia..., architecturalviewofm..., and the system clock is 6:41 PM.

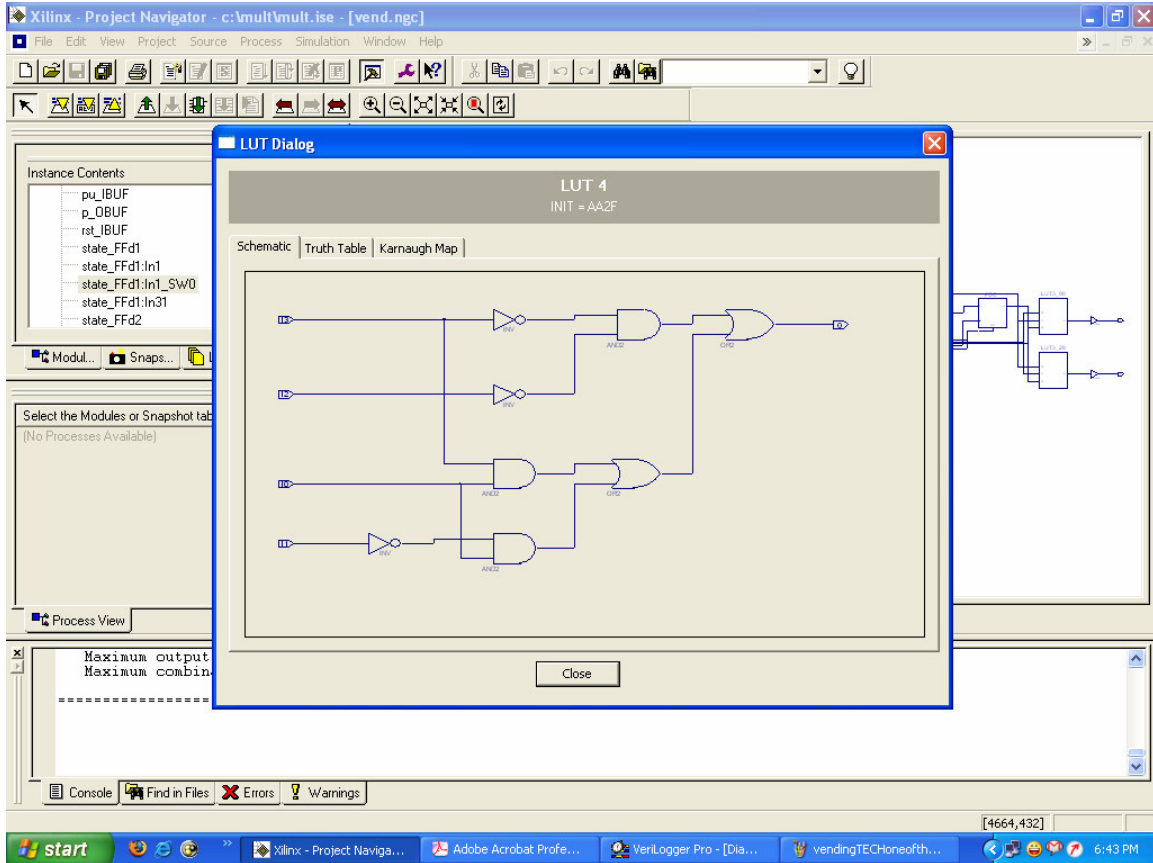
Technology Schematic:

The screenshot displays the Xilinx Project Navigator interface. The main window shows a top-level schematic diagram with various logic blocks and interconnections. The console window at the bottom displays the following text:

```
Maximum output required time after clock: 10.502ns  
Maximum combinational path delay: No path found  
.....
```

The interface includes a menu bar (File, Edit, View, Project, Source, Process, Simulation, Window, Help), a toolbar, and several panels: Instance Contents (listing Pins, Nets, Instances), Select the Modules or Snapshot tab (No Processes Available), and a Process View section. The bottom status bar shows the file path [3598, 1286] and the system clock 6:42 PM.

One of the blocks of Technology Schematic



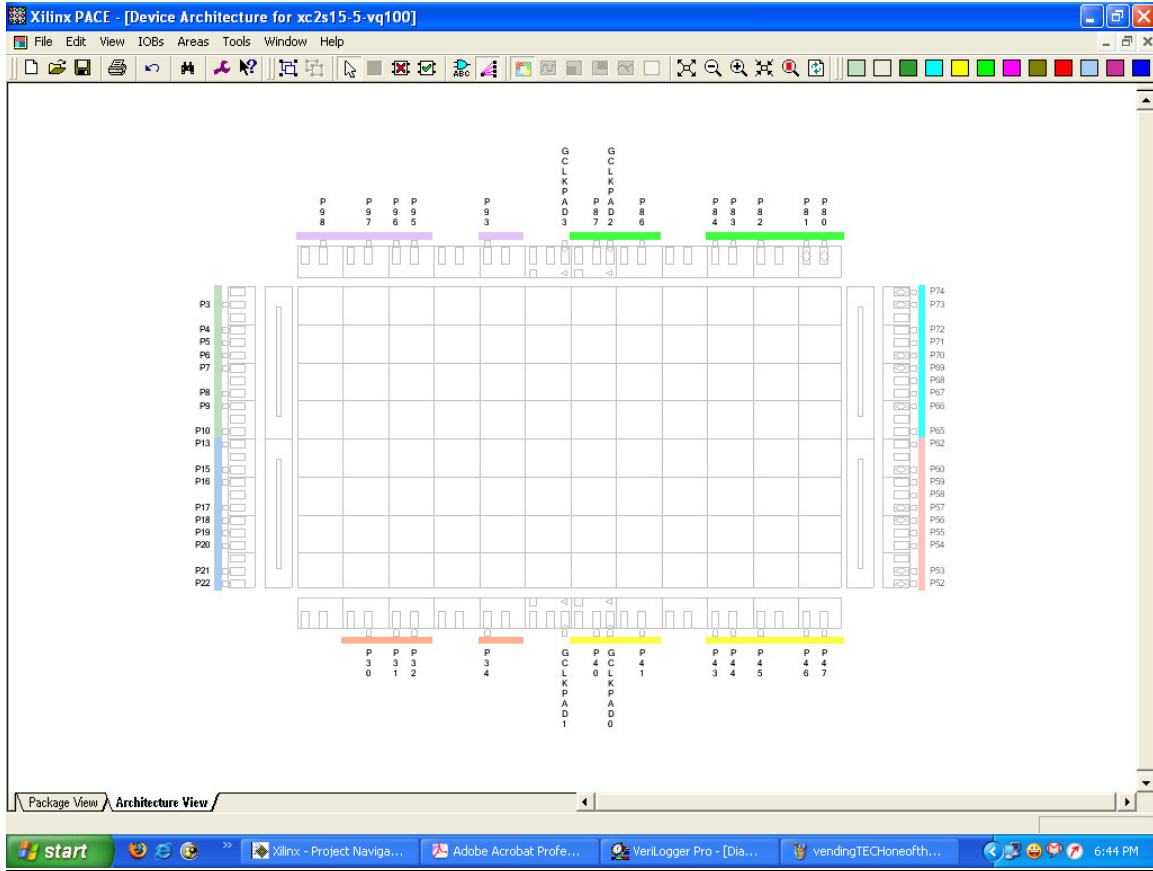
K-Map of the above block

The screenshot shows the Xilinx Project Navigator interface with the LUT Dialog window open. The dialog displays the Karnaugh Map for LUT 4 (INIT = AA2F). The K-Map is a 4x4 grid with inputs 00, 01, 11, 10 and outputs 00, 01, 11, 10. The values are 1, 0, 0, 0 for 00; 1, 0, 0, 0 for 01; 1, 1, 1, 0 for 11; and 1, 1, 1, 1 for 10.

	00	01	11	10
00	1	0	0	0
01	1	0	0	0
11	1	1	1	0
10	1	1	1	1

The dialog also shows the Instance Contents on the left, including pu_IBUF, p_OBUF, rst_IBUF, state_FFd1, state_FFd1.in1, state_FFd1.in1_SW0, state_FFd1.in31, and state_FFd2. The bottom status bar shows the console, find in files, errors, and warnings sections.

ARCHITECTURE VIEW:



SYNTHESIS REPORT:

The screenshot shows the Xilinx Project Navigator interface. The main window displays the 'Design Summary' for the project 'vend'. The interface includes a 'Sources in Project' pane on the left, a 'Processes for Source' pane, and a central 'Design Overview' pane. At the bottom, there is a console window showing the synthesis process output.

Sources in Project:

- mult.isc
- xc2s15-5vq100
 - vend (.vend.v)
 - vend.ucf

Design Overview for vend

Property	Value
Project Name:	c:\mult
Target Device:	xc2s15
Report Generated:	Tuesday 04/11/06 at 18:41
Printable Summary (View as HTML):	vend_summary.htm

Device Utilization Summary (estimated values)

Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slices:	6	192	3%	
Number of Slice Flip Flops:	3	384	0%	
Number of 4 input LUTs:	11	384	2%	
Number of bonded IOBs:	7	64	10%	
Number of GCLKs:	1	4	25%	

Performance Summary

Property	Value
Data Not Yet Available	

Failing Constraints

Constraint(s)	Requested	Actual	Logic Levels
Data Not Yet Available			

Detailed Reports

Report Name	Status	Last Date Modified
Synthesis Report	Current	Tuesday 04/11/06 at 18:41

Console Output:

```

Number of warnings: 0
Writing NGD file "vend.ngd" ...
Writing NGDBUILD log file "vend.bld" ...
NGDBUILD done.
  
```

The Windows taskbar at the bottom shows the system time as 8:13 PM on 04/11/06.

COMPILATION:

Release 7.1i - xst H.38

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--> Parameter TMPDIR set to __projnav

CPU : 0.00 / 0.67 s | Elapsed : 0.00 / 1.00 s

--> Parameter xsthdpdir set to ./xst

CPU : 0.00 / 0.67 s | Elapsed : 0.00 / 1.00 s

--> Reading design: vend.prj

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 - 7.1) Device utilization summary
 - 7.2) TIMING REPORT

```
=====
*           Synthesis Options Summary           *
=====
```

---- Source Parameters

Input File Name : "vend.prj"
Input Format : mixed
Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "vend"
Output Format : NGC
Target Device : xc2s15-5-vq100

---- Source Options

Top Module Name : vend
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
FSM Style : lut
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
ROM Style : Auto

Mux Extraction : YES
Decoder Extraction : YES
Priority Encoder Extraction : YES
Shift Register Extraction : YES
Logical Shifter Extraction : YES
XOR Collapsing : YES
Resource Sharing : YES
Multiplier Style : lut
Automatic Register Balancing : No

---- Target Options

Add IO Buffers : YES
Global Maximum Fanout : 100
Add Generic Clock Buffer(BUFG) : 4
Register Duplication : YES
Equivalent register Removal : YES
Slice Packing : YES
Pack IO Registers into IOBs : auto

---- General Options

Optimization Goal : Speed
Optimization Effort : 1
Keep Hierarchy : NO
Global Optimization : AllClockNets
RTL Output : Yes
Write Timing Constraints : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : maintain
Slice Utilization Ratio : 100
Slice Utilization Ratio Delta : 5

---- Other Options

lso : vend.lso
Read Cores : YES
cross_clock_analysis : NO
verilog2001 : YES
safe_implementation : No
Optimize Instantiated Primitives : NO
tristate2logic : Yes
use_clock_enable : Yes
use_sync_set : Yes
use_sync_reset : Yes
enable_auto_floorplanning : No

=====

* HDL Compilation *

```
=====  
Compiling verilog file "../vend.v"  
Module <vend> compiled  
No errors in compilation  
Analysis of file <"vend.prj"> succeeded.  
=====
```

* HDL Analysis *

```
=====  
Analyzing top module <vend>.  
  S0 = <u>000  
  S1 = <u>001  
  S2 = <u>010  
  S3 = <u>011  
  S4 = <u>100  
  S5 = <u>101  
  S6 = <u>110  
  S7 = <u>111  
Module <vend> is correct for synthesis.  
=====
```

* HDL Synthesis *

```
=====  
Synthesizing Unit <vend>.  
  Related source file is "../vend.v".  
INFO:Xst:1799 - State 111 is never reached in FSM <state>.  
  Found finite state machine <FSM_0> for signal <state>.  
-----
```

States	7	
Transitions	16	
Inputs	3	
Outputs	6	
Clock	clk (rising_edge)	
Reset	rst (negative)	
Reset type	asynchronous	
Reset State	000	
Encoding	automatic	
Implementation	LUT	

```
-----  
Summary: inferred 1 Finite State Machine(s).  
Unit <vend> synthesized.  
=====
```

* Advanced HDL Synthesis *

```
=====  
Advanced RAM inference ...  
Advanced multiplier inference ...  
=====
```

Advanced Registered AddSub inference ...
Analyzing FSM <FSM_0> for best encoding.
Optimizing FSM <FSM_0> on signal <state[1:3]> with gray encoding.

State | Encoding

000 | 000
010 | 001
001 | 011
101 | 010
011 | 110
110 | 111
100 | 101
111 | unreachable

Dynamic shift register inference ...

=====

HDL Synthesis Report

Macro Statistics

FSMs : 1
Registers : 3
1-bit register : 3

=====

* Low Level Synthesis *

=====

Optimizing unit <vend> ...

Loading device for application Rf_Device from file '2s15.nph' in environment C:/Xilinx.

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block vend, actual ratio is 3.

=====

* Final Report *

=====

Final Results

RTL Top Level Output File Name : vend.ngr
Top Level Output File Name : vend
Output Format : NGC
Optimization Goal : Speed

Keep Hierarchy : NO

Design Statistics

IOs : 7

Cell Usage :

BELS : 13
INV : 1
LUT2 : 2
LUT3 : 2
LUT3_L : 2
LUT4 : 1
LUT4_L : 4
MUXF5 : 1
FlipFlops/Latches : 3
FDC : 3
Clock Buffers : 1
BUFGP : 1
IO Buffers : 6
IBUF : 4
OBUF : 2

=====

Device utilization summary:

Selected Device : 2s15vq100-5

Number of Slices: 6 out of 192 3%
Number of Slice Flip Flops: 3 out of 384 0%
Number of 4 input LUTs: 11 out of 384 2%
Number of bonded IOBs: 7 out of 64 10%
Number of GCLKs: 1 out of 4 25%

=====

TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE
REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

Clock Signal	Clock buffer(FF name)	Load
clk	BUFGP	3

Timing Summary:

Speed Grade: -5

Minimum period: 6.351ns (Maximum Frequency: 157.456MHz)
Minimum input arrival time before clock: 7.866ns
Maximum output required time after clock: 10.502ns
Maximum combinational path delay: No path found

Timing Detail:

All values displayed in nanoseconds (ns)

Timing constraint: Default period analysis for Clock 'clk'

Clock period: 6.351ns (frequency: 157.456MHz)

Total number of paths / destination ports: 12 / 3

Delay: 6.351ns (Levels of Logic = 2)

Source: state_FFd2 (FF)

Destination: state_FFd3 (FF)

Source Clock: clk rising

Destination Clock: clk rising

Data Path: state_FFd2 to state_FFd3

Cell:in->out	Gate	Net	fanout	Delay	Delay	Logical Name (Net Name)
FDC:C->Q	6	1.292	1.850	state_FFd2	(state_FFd2)	
LUT4:I0->O	1	0.653	1.150	state_FFd3-In1_SW1	(N15)	
LUT4_L:I2->LO	1	0.653	0.000	state_FFd3-In1	(state_FFd3-In)	
FDC:D	0.753			state_FFd3		

Total 6.351ns (3.351ns logic, 3.000ns route)
(52.8% logic, 47.2% route)

Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'

Total number of paths / destination ports: 16 / 3

Offset: 7.866ns (Levels of Logic = 4)
Source: i (PAD)
Destination: state_FFd3 (FF)
Destination Clock: clk rising

Data Path: i to state_FFd3

Cell:in->out	Gate	Net	fanout	Delay	Delay	Logical Name (Net Name)

IBUF:I->O	4	0.924	1.600	i_IBUF	(i_IBUF)	
LUT2:I0->O	3	0.653	1.480	state_FFd2-In31	(N5)	
LUT4:I3->O	1	0.653	1.150	state_FFd3-In1_SW1	(N15)	
LUT4_L:I2->LO	1	0.653	0.000	state_FFd3-In1	(state_FFd3-In)	
FDC:D	0.753			state_FFd3		

Total		7.866ns	(3.636ns logic, 4.230ns route)			(46.2% logic, 53.8% route)

=====
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
Total number of paths / destination ports: 6 / 2

Offset: 10.502ns (Levels of Logic = 2)
Source: state_FFd1 (FF)
Destination: c (PAD)
Source Clock: clk rising

Data Path: state_FFd1 to c

Cell:in->out	Gate	Net	fanout	Delay	Delay	Logical Name (Net Name)

FDC:C->Q	6	1.292	1.850	state_FFd1	(state_FFd1)	
LUT3:I0->O	1	0.653	1.150	_n00001	(p_OBUF)	
OBUF:I->O	5.557			p_OBUF	(p)	

Total		10.502ns	(7.502ns logic, 3.000ns route)			(71.4% logic, 28.6% route)

=====
CPU : 3.81 / 4.53 s | Elapsed : 4.00 / 5.00 s
Total memory usage is 82268 kilobytes

Number of errors : 0 (0 filtered)
Number of warnings : 0 (0 filtered)
Number of infos : 1 (0 filtered)