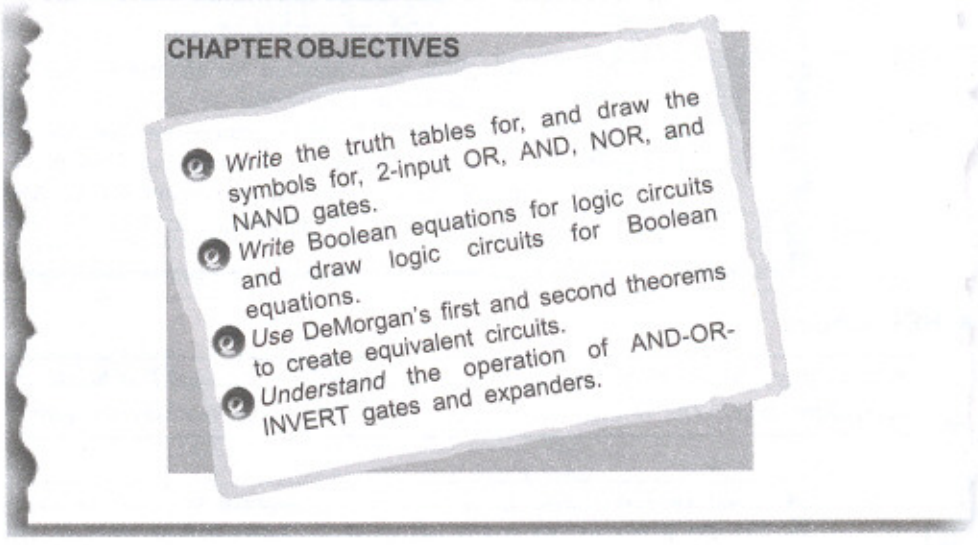
Guided Tour

• Chapter Objectives

Chapter Objectives provide a quick look into the concepts that will be discussed in the chapter.



• Examples

Every chapter contains several worked out examples which will guide the students while understanding the concepts and working out the exercise problems.

EXAMPLE 4.1

Show how 4-to-1 multiplexer can be obtained using only 2-to-1 multiplexer.

Solution

Logic equation for 2-to-1 Multiplexer: $Y = A'.D_0 + A.D_1$

Logic equation for 4-to-1 Multiplexer: $Y = A'B'.D_0 + A'B.D_1 + AB'.D_2 + AB.D_3$

This can be rewritten as, $Y = A'(B'.D_0 + B.D_1) + A(B'.D_2 + B.D_3)$

Compare this with equation of 2-to-1 multiplexer. We need two 2-to-1 multiplexer to realize two bracketed terms where B serves as select input. The output of these two multiplexers can be sent to a third multiplexer as data inputs where A serves as select input and we get the 4-to-1 multiplexer. Figure 4.8a shows circuit diagram for this.

• Self-Test

A section called Self-Test appears after every section in every chapter of the book. These will help students in checking their understanding of the concepts discussed in a section before moving on to the next section. Answers to Self-Tests in a chapter are given at the end of that chapter.

SELF-TEST

4. Write an expression for an inverter, or NOT gate equivalent to Y = not A.
5. Write a Boolean expression for an OR gate having A and B as inputs and Y as the output.
6. Write the Boolean expression for an AND gate with A and B as inputs and Y as the output.

• HDL Codes

New to this edition, HDL, an interesting development in the field of hardware design, has been introduced. The relevant HDL description and codes are weaved into chapters.

```
module DLatch(D,EN,Q);
input D,EN;
output Q;
reg Q;
always @ (EN or D)
   if (EN) Q=D;
  //from characteristic equation
endmodule
```

```
module SRLatch(S,R,EN,Q);
input S,R,EN;
output Q;
reg Q;
always @ (EN or S or R)
   if (EN) Q=S|(~R&Q);
  //from characteristic equation
endmodule
```

• Figures

Figures are used exhaustively in the text to illustrate the concepts and methods described.

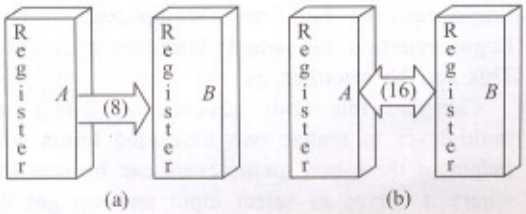


Fig. 1.19 *(a) An 8-bit data bus. (b) A 16-bit, bidirectional data bus.*

• Summary

Summary gives the essence of each chapter in brief and will be helpful for a quick review during the examinations.

SUMMARY

Almost all digital circuits are designed for two-state operation, which means the signal voltages are either at a low level or a high level. Because they duplicate mental processes, digital circuits are often called logic circuits. A gate is a digital circuit with 1 or more inputs, but only 1 output. The output is high only for certain combinations of the input signals.

• Problems

The text contains more than 500 exercise problems for the students to work out and practice. This will help them in improving their problem-solving skills.

PROBLEMS

Section 4.1

4.1 In Fig. 4.2, if $ABCD$ = 1001, what does Y equal?

4.2 In Fig. 4.4, if $ABCD$ = 1100, what does Y equal?

4.3 We want to implement Table 3-12 of the preceding chapter using multiplexer logic. Show a circuit, similar to the one in Fig. 4.4, that can do the job.

4.4 Show how to connect a 74150 to implement this Boolean equation:

$$Y = \overline{A}B\overline{C}D + A\overline{B}C\overline{D} + ABC\overline{D}$$

• Glossary

Glossary listed at the end of each chapter gives the important definitions discussed in the chapter. It also lists the abbreviations used in the chapter.

GLOSSARY

- ***active-low*** Active-low refers to the concept in which a signal must be low to cause something to happen or to indicate that something has happened.
- ***AND gate*** A gate with 2 or more inputs. The output is high only when all inputs are high.
- ***assert*** To activate. If an input line has a bubble on it, you assert the input by making it low. If there is no bubble, you assert the input by making it high.

• Web site

A dedicated Web site for the book at http://www.mhhe.com/leach/dpa6 has solutions to selected problems given at the end of the chapters and PowerPoint slides for the instructors. For the students, some experiments for selected chapters are available. Also Quine-McClusky computer codes and HDL codes of a Multiplier are there for the students in the accompanying Web site, which will be updated from time to time. Students will also have access to additional reading material on the topics of error detection and correction and five variable K-map.