Preface to the Third Edition

Motivation for a Third Edition

Since the publication of the second edition over 15 years ago, the integrated circuit (IC) industry has undergone a tremendous amount of change. The most significant trend is the emergence of CMOS as the dominant IC technology. Other technologies such as NMOS, bipolar, and GaAs, have given way to CMOS due to considerations such as power, level of integration, and cost. The tools, technologies, and know-how in CMOS are so pervasive that it will continue to lead the industry for the next decade.

A second important trend is that scaling is continuing its relentless pace according to Moore's Law. The industry reached the 1 μm minimum line width around the time of publication of the second edition. This was once considered to be a physical and psychological limit of scaling. However, it was quickly realized that transistors could be fabricated with minimum dimensions well below 1 μm and this ushered in the submicron era. Since then, we have been witness to six generations of technology scaling: 0.8 μm, 0.5 μm, 0.35 μm, 0.25 μm, 0.18 μm, and 0.13 μm.

At roughly the 0.35 μm technology node, we entered the deep submicron era where a number of fundamental changes were encountered in behavior of transistors and wires. Devices experienced a number of short-channel effects, perhaps the most important of which is velocity saturation. Interconnect began to control many of the electrical properties of the design such as delay, noise, power, and reliability. As a result, the transition from 0.18 μm to 0.13 μm also triggered a wholesale switch from aluminum to copper to mitigate these new interconnect issues. With all of these fundamental changes in the IC industry, there was a need to completely revise this book.

What's in the New Edition?

- We have focused on CMOS technology and moved the bipolar material to an Appendix.
- The content is based on 0.18 μm and 0.13 μm CMOS technologies.

- Most recent CMOS fabrication processes are described, including shallow-trench isolation, copper interconnect, and low-*k* dielectrics.
- Two important chapters have been added on deep submicron interconnect.
- New material has been added on logical effort that is useful for back-of-the-envelope calculations of optimal gates sizes in high-speed CMOS design.
- Advanced material has also been added on Flash memories, field-programmable gate arrays, and content-addressable memories.
- A chapter has been added on advanced power grid design, clock design, and phase-locked loops.
- A new section has been added on BSIM3 modeling and simulation.
- This edition uses short-channel MOS device equations with velocity saturation throughout the book. New equations have been derived for noise margins and switching thresholds.
- Junction capacitance modeling has been updated to include shallow-trench isolation effects.
- A SPICE tutorial has been provided in Appendix A.
- Gallium arsenide has been removed from this edition.

With these changes, the new edition of the book will be valuable for many years to come.

Why Buy This Book?

This book will teach you how to think like a designer. It is the product of the design know-how of many of the leaders in the field. This edition also contains extremely valuable information for practicing engineers in the semiconductor industry. The real value of the book is that it starts with the fundamentals of semiconductor devices and sequences in a step-by-step fashion to the key issues of digital IC design in deep submicron technologies. Like the previous editions, it is intended to be used as a fourth-year university textbook, with some of the latter material suitable for first-year graduate courses.

This book retains the readability and accessibility of previous editions that led to its widespread use. While the goal is to provide the reader with the key concepts and equations for digital IC design, it provides much more detail than other books in the field. Concepts are introduced in a logical sequence and then reinforced throughout the book. Complex equations are reduced to simple design equations that can be used to carry out rapid hand calculations.

There are many derivations, worked examples, exercises, and SPICE simulations to allow the student and practicing engineer to build a solid understanding of the material in each chapter. There are problems at the back of the chapter to gain experience with the material and explore other topics not directly covered in the chapter. The chapter summaries are in the form of useful equations and parameters from each chapter. The inside front and back covers provide useful parameters, scale factors, and conversion factors that are used throughout the book.

Website for the Book

A website for the textbook is available through McGraw-Hill. The website contains solutions, supporting material, color diagrams, illustrations, design problems, and errata. The website is valuable in constructing lecture material for a course based on this book.

Advanced CMOS Technologies

The material in this book is built around the 0.18 μm and 0.13 μm technology nodes. Both technologies are covered in enough detail to select one or the other as the primary technology for a course based on this book. Since SPICE is the simulation tool used in this book, it is necessary to have access to device models for one of these two technologies for the course. All of the SPICE examples are based on 0.18 μm, while the worked problems are based on both 0.18 μm and 0.13 μm technologies. The textbook is also suitable for technologies below 0.13 μm, with appropriate changes in the examples and problems at the back of the chapters.

Advanced Topics

Advanced topics are included for students wishing to go beyond the basic material of this text and gain insight into the issues in industry. They are designated with an asterisk ($\star$) and may be skipped without loss of continuity.

How to Use This Book

Chapters 1–3 comprise the foundational material upon which the rest of the book is based. Chapters 4–7 are the main body of the text where all of the transistor-level design issues are described in detail. Chapter 8 focuses on an application of all material covered in the book, specifically in static memory design. Chapter 9 describes advanced topics in semiconductor memory design. The book continues with a detailed treatment of deep submicron interconnect issues in Chapter 10 and concludes with power grid and clock design in Chapter 11.

For a 15-week semester course, with 3 hours of lecture time each week, the entire text may be covered at the rate of about one chapter each week. For a 12-week course, there is sufficient time to cover Chapters 1–8, Chapter 10, and selected topics in Chapters 9 and 11.

In a 10-week course, only Chapters 1–8 and Chapter 10 can be covered assuming that much of the advanced topics are skipped. Depending on the background of the students entering the course, instructors should use their own discretion in selecting the appropriate material and sequencing of this book.

A chapter-by-chapter outline of the topics follows.

Chapter 1
Deep Submicron Digital IC Design
In the first chapter, we provide a perspective on digital design in the deep submicron era and motivate the topics in the rest of the book. We briefly review important concepts of logic gates primarily to provide notational context for the book, including the ideal logic element, static input-output characteristics, noise margin, and propagation delay time. Then we elaborate on the key issues in deep submicron such as power dissipation, velocity saturated transistors, interconnect resistance, coupling capacitance, and inductance. The role of computer-aided design tools such as SPICE is described. The chapter concludes with the challenges ahead as described in the technology roadmap.

Chapter 2
MOS Transistors
The short-channel device models to be used in the rest of this book are described in this chapter. To begin the treatment, rudimentary device physics concepts are covered to explain the threshold voltage equation and the transistor current equations. Both long- and short-channel models are derived. Then the oxide and junction capacitance models are described to complete the chapter.

Chapter 3
Fabrication, Layout, and Simulation
This chapter describes the relationship between fabrication, layout, and simulation in the integrated circuit design process. The topics of fabrication and layout are important to IC designers and should be well-understood. However, for this course, it serves more as a background for the rest of the text. The more important subject is simulation with SPICE. The model parameters for SPICE are detailed in this chapter. A brief user manual is provided in Appendix A for those unfamiliar with the basics of SPICE. We also provide some advanced material on MOS transistors and fabrication technologies of the future.

Chapter 4
MOS Inverter Circuits
This is a core chapter on MOS digital inverters and introduces concepts of voltage transfer characteristics, noise margins, inverter configurations, and simple timing and power calculations. Analytical equations are derived for noise margin parameters and switching thresholds of inverters for a number of MOS inverters.

Chapter 5
Static MOS Gate Circuits
This is another core chapter of the book. It examines the static design issues for NANDs, NORs, and complex gates. It develops extensions to inverter design to size the transistors in CMOS gates. Sequential elements, such as flip-flops and latches, are described in this chapter. The chapter concludes with a detailed treatment of the various components of power dissipation in logic gates.

Chapter 6
High-Speed CMOS Logic Design
This chapter describes the issues involved in high-speed logic design. It develops useful equations for switching delay calculation for step and ramp inputs. This involves the use of the large-signal on-resistance of gates, and the calculation of the loading capacitance, both of which are detailed. The total capacitance can be computed using two key parameters for input and output capacitance. Gate sizing for equal delay and minimal delay are described. The thrust of the latter half of this chapter is high-speed logic optimization using logical effort.

Chapter 7
Transfer Gate and Dynamic Logic Design
In this chapter, we explore dynamic design techniques using transmission gates and precharged logic. The important concepts of charge-sharing, bootstrapping, feedthrough, and charge leakage are elaborated in this chapter. Domino logic is described in detail as it is the most common form of dynamic logic in use today. These concepts lay the groundwork for the operation of many of the memory circuits discussed in the next two chapters.

Chapter 8
Semiconductor Memory Design
This chapter addresses the analysis and design of VLSI memories, commonly known as semiconductor memories. In this chapter, we classify the different types of memory, examine the major subsystems, and then focus on the static RAM (SRAM) design issues. This topic is particularly suitable for our study of CMOS digital design as it allows us to apply many of the basic concepts presented in earlier chapters. The entire design process for static RAMs is described in detail.

Chapter 9
Additional Topics in Memory Design
This chapter explores a variety of other semiconductor memories, their architectures, access mechanisms, and cell configurations. We begin by examining content-addressable memories, since they are a derivative of the SRAM architecture. We also cover an important application of SRAM cells in the growing market segment of programmable logic called field-programmable gate-arrays (FPGAs). The chapter sequences through dynamic RAMs, mask-programmable ROMs, erasable programmable ROMs, electrically-erasable ROMs and Flash memories, and concludes with a look at memory cells based on ferroelectric materials called FRAMs.

Chapter 10
Interconnect Design
This chapter is devoted to the study of interconnect issues that the IC designer faces when designing in deep submicron technologies. It addresses the issues associated with *RLC* aspects of wires in detail. We begin by re-examining the *RC* delay calculation using the Elmore delay, and address the issue of buffer insertion in long wires.

Then we examine the capacitances associated with 3D interconnect which leads to a discussion of the effect of coupling capacitance on delay and crosstalk in logic circuits. The chapter continues with a discussion of inductance effects, and concludes with a look at antenna effects.

Chapter 11
Power Grid and Clock Design
In this chapter, we address two chip-level design issues that are dominated by interconnect: power system distribution and clock distribution. This chapter addresses advanced issues such as power routing, *IR* drop, *Ldi*/*dt*, and the impact of voltage drop on timing. The chapter highlights the interaction of the power system with the clock design. It also addresses clock generation and phase-lock loop (PLL) circuits to conclude the chapter.

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