Do any 11 of the 12 problems. Each is worth 20 points. Make sure it is clear which problem you do not want graded or I will grade the first 11 on which anything is written.

1.   Show the state table or state diagram for a Mealy system that produces a 1 output if and only if the last 6 inputs have been 0 1 0 0 1 0. You may allow overlapping or not, but must indicate which. (6 states)

```
x:          1  1  0  1  0  0  1  0  0  1  0  1  0  0  1  0
z overlap:  0  0  0  0  0  0  0  1  0  0  1  0  0  0  0  1  0
z not:      0  0  0  0  0  0  0  1  0  0  0  0  0  0  0  1  0
```

2.   For the following state table and state assignments, design a system, using one T and one JK flip flop.

q	q *		z
	x = 0	x = 1	
A	C	B	1
B	C	A	0
C	B	D	0
D	D	A	0

| q	q_1	q_2
A	0	0
B	0	1
C	1	1
D	1	0

Show equations for the flip flop inputs and the system output. Maximum credit for the design using the minimum amount of combinational logic (AND, OR and NOT gates). You must decide which flip flop is JK and which is T.

3.   DO EITHER a or b; 5 point bonus for both.

a.   We want to design a Mealy system that produces an output of 1 if and only if the last 6 inputs are 0 1 0 1 0 1 or the output is 1 and the input is continuing on that pattern. In addition to AND, OR and NOT gates, we have available an 8-bit serial-in, parallel-out shift register, with an active low, clocked clear.

x   0 0 1 0 1 0 1 0 1 0 0

z   ? 0 0 0 0 0 1 1 1 1 0 0 0
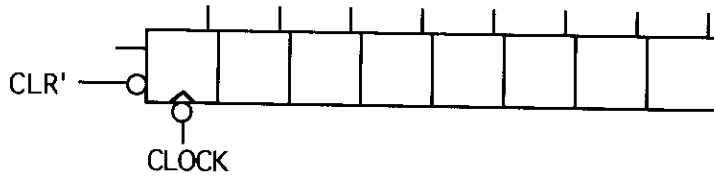
b.   We want to design a Moore system with an output of 1 if and only if the input has been 1 for 7 or more consecutive clock times. In addition to AND, OR and NOT gates, we have available a 4-bit counter with an active low clocked clear (that works whether or not the counter is enabled), and an active low enable.
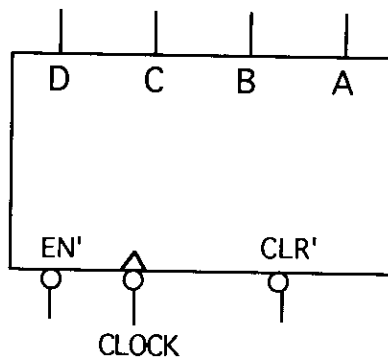
4.   For the following circuit, complete state table and the timing diagram below (for A, B and z), as far as you can go. Assume A and B are intially 0.
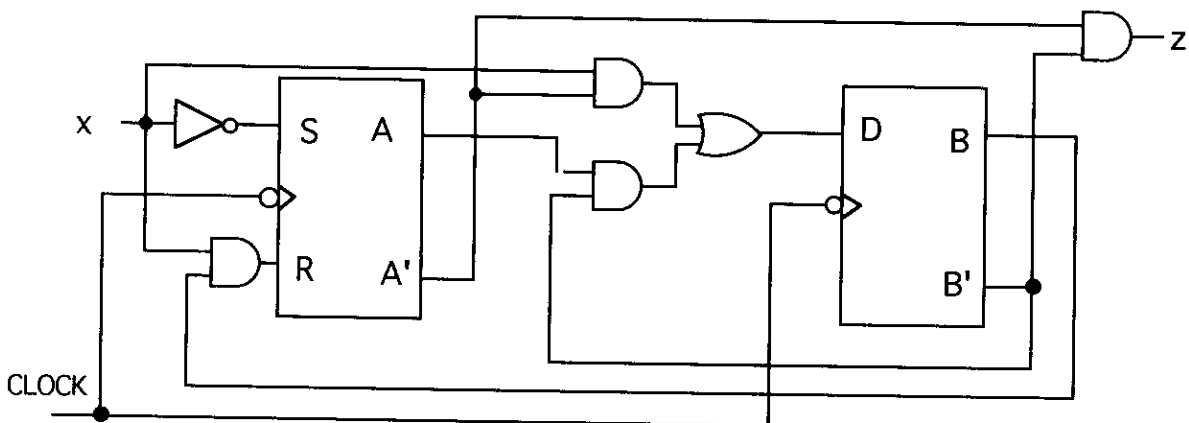
A B	A* B*		z
	x = 0	x = 1	
0 0			
0 1			
1 0			
1 1			

CLOCK

x

A

B

z
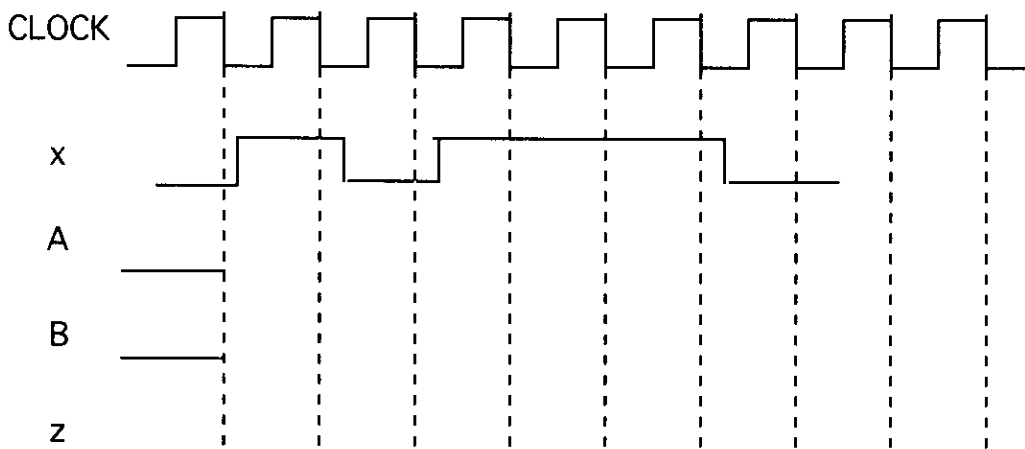
5.   for the following circuit, complete the timing trace as far as you can, even after you no longer know the input.

J	A		D	B		S	C		T	D
K	A'			B'		R	C'			D'

x   ⌐   CLOCK

x	0	1	1	0	1	0	1
A	0						
B	0						
C	0						
D	0						
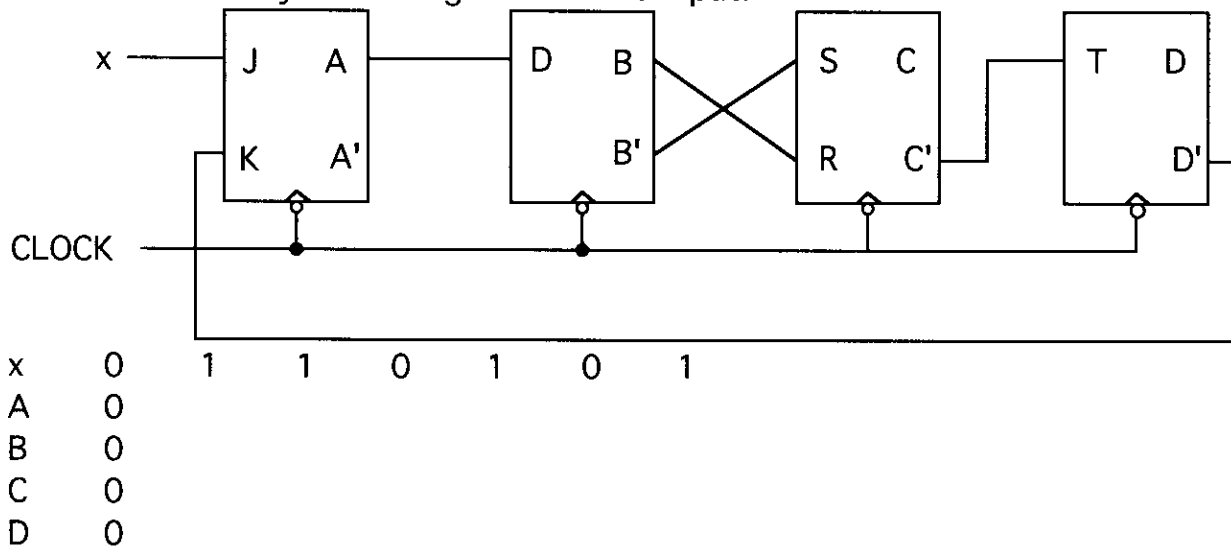
6. Design a counter that goes through the sequence

        1   3   5   6   4   2   and repeat

using JK flip flops.

Show a state diagram, including what happens if the system is initially in one of the unused states (0, 7).

7. For the following system

q	q^*	
	x = 0	x = 1
A	D	B
B	C	D
C	E	D
D	A	B
E	E	D

    a)   Find all SP partitions.
    b)   Show an output column for a Moore system that allows you to reduce this to three stastes (but not two or one) and show the reduced table.

8. For the following function, find

    a)   both minimum sum of products expressions
    b)   both minimum product of sums expressions

Assume all inputs are available both uncomplemented and complemented.

$$f(a, b, c, d) = \sum m(1, 3, 6, 9, 11, 12, 14) + \sum d(2, 15)$$

5-point bonus: Which, if any of the solutions are equal?

9. For the following 5-variable problem, find the 6 minimum solutions. Each has 5 terms and 16 literals. (Three copies of the map are given.)

A

Map A = 0 — columns BC, rows DE:

DE \ BC	00	01	11	10
00	1		X	1
01	X			1
11				1
10	X	1		1

Map A = 1 — columns BC, rows DE:

DE \ BC	00	01	11	10
00			X	
01	1		1	1
11	1			1
10	1	X		

10. For the following three functions, find a minimum sum of product solution, treating each as a separate problem. Assume all inputs are available both uncomplemented and complemented. Indicate the number of gates and gate inputs that would be required for a two-level NAND gate solution. Do NOT draw the circuit.

Map f — columns wx, rows yz:

yz \ wx	00	01	11	10
00	1	1	1	
01	1			
11		1		
10	1	1	1	1

f

Map g — columns wx, rows yz:

yz \ wx	00	01	11	10
00	1	1	1	
01	1			1
11	1	1		1
10	1			

g

Map h — columns wx, rows yz:

yz \ wx	00	01	11	10
00	1	1	1	
01	1	1	1	
11		1		
10	1			

h

11. For the following three functions, find a minimum two-level solution corresponding to an AND/OR solution. Minimum is minimum number of gates and among those with the same number of gates, minimum number of gate inputs. (10 gates, 31 inputs) Assume all inputs are available both uncomplemented and complemented. (Note that these are the same functions as in problem 11.) Only the equations and the maps (with terms circled) are required.

Map f (wx across: 00 01 11 10; yz down: 00 01 11 10)

yz \ wx	00	01	11	10
00	1	1	1	
01	1			
11		1		
10	1	1	1	1

f

Map g (wx across: 00 01 11 10; yz down: 00 01 11 10)

yz \ wx	00	01	11	10
00	1	1	1	
01	1			1
11	1	1		1
10	1			

g

Map h (wx across: 00 01 11 10; yz down: 00 01 11 10)

yz \ wx	00	01	11	10
00	1	1	1	
01	1	1	1	
11		1		
10	1			

h

12.   Find an implementation of the following function (already in minimum sum of product form) using only two-input NAND gates. Assume all inputs are available both uncomplemented and complemented. Show both the equation and the block diagram.   (10 two-input gates for full credit)

$$f = a'cde + a'be + bc' + ab'e + ab'cd$$