transistors acting in the switched-mode). A 555-timer chip drives the two inputs, which are the timer's clock (CLK), and its inverse, clock-not$(\overline{CLK})$. $\overline{CLK}$ is low whenever CLK is high, and conversely. Assuming that the frequency of the clock is relatively high, determine the voltage across a high resistance load, R.

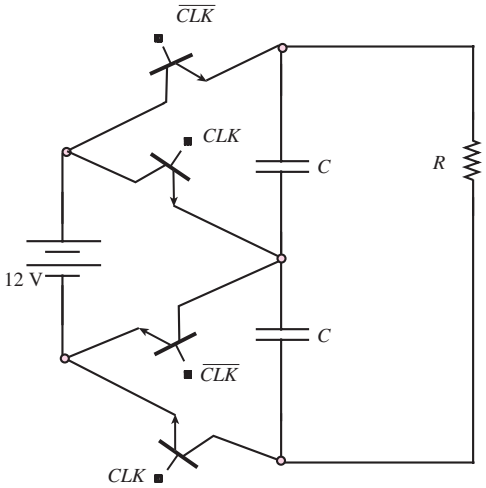


Figure P12.36

12.37 Sketch the low-power periodic signals, A, B, and C vs. *time,* that drive the high current power transistors in the (DC)-to-(three-phase-AC) switched mode power supply of Figure P12.37, so that the load sees a balanced three-phase square-wave source.

In Figure P12.37 the right switches should be labeled $\overline{A}\ \overline{B}\ \overline{C}$

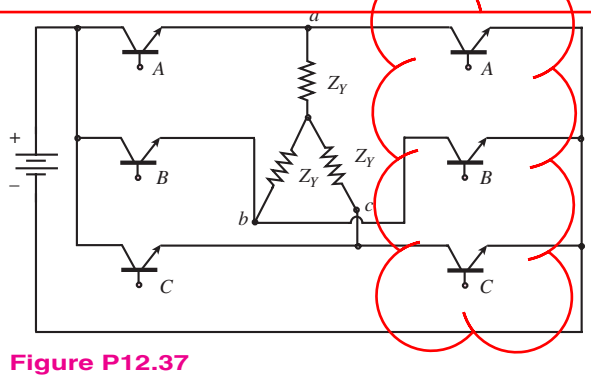
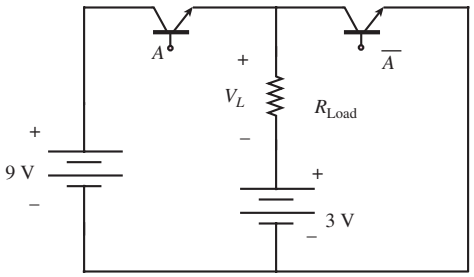


Figure P12.37

12.38 In the switched mode power supply of Figure P12.38, sketch the load voltage signal, V_L.



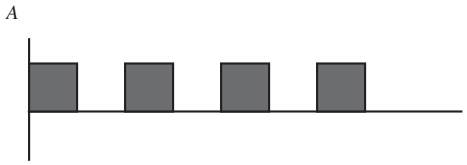


Figure P12.38