We now apply KVL to the branches involving the voltage sources as shown in Fig. 3.13(b). For loop 1,

$$-v_1 + 20 + v_2 = 0 \qquad \Rightarrow \qquad v_1 - v_2 = 20 \tag{3.4.3}$$

For loop 2,

$$-v_3 + 3v_x + v_4 = 0$$

But $v_x = v_1 - v_4$ so that

$$3v_1 - v_3 - 2v_4 = 0 \tag{3.4.4}$$

For loop 3,

$$v_x - 3v_x + 6i_3 - 20 = 0$$

But $6i_3 = v_3 - v_2$ and $v_x = v_1 - v_4$. Hence

$$-2v_1 - v_2 + v_3 + 2v_4 = 20 \tag{3.4.5}$$

We need four node voltages, $v_1, v_2, v_3$, and $v_4$, and it requires only four out of the five Eqs. (3.4.1) to (3.4.5) to find them. Although the fifth equation is redundant, it can be used to check results. We can solve Eqs. (3.4.1) to (3.4.4) directly using *MATLAB*. We can eliminate one node voltage so that we solve three simultaneous equations instead of four. From Eq. (3.4.3), $v_2 = v_1 - 20$. Substituting this into Eqs. (3.4.1) and (3.4.2), respectively, gives

$$6v_1 - v_3 - 2v_4 = 80 \tag{3.4.6}$$

and

$$6v_1 - 5v_3 - 16v_4 = 40 \tag{3.4.7}$$

Equations (3.4.4), (3.4.6), and (3.4.7) can be cast in matrix form as

$$\begin{bmatrix} 3 & -1 & -2 \\ 6 & -1 & -2 \\ 6 & -5 & -16 \end{bmatrix} \begin{bmatrix} v_1 \\ v_3 \\ v_4 \end{bmatrix} = \begin{bmatrix} 0 \\ 80 \\ 40 \end{bmatrix}$$

Using Cramer's rule gives

$$\Delta = \begin{vmatrix} 3 & -1 & -2 \\ 6 & -1 & -2 \\ 6 & -5 & -16 \end{vmatrix} = -18, \qquad \Delta_1 = \begin{vmatrix} 0 & -1 & -2 \\ 80 & -1 & -2 \\ 40 & -5 & -16 \end{vmatrix} = -480$$

$$\Delta_3 = \begin{vmatrix} 3 & 0 & -2 \\ 6 & 80 & -2 \\ 6 & 40 & -16 \end{vmatrix} = -3120, \qquad \Delta_4 = \begin{vmatrix} 3 & -1 & 0 \\ 6 & -1 & 80 \\ 6 & -5 & 40 \end{vmatrix} = 840$$

Thus, we arrive at the node voltages as

$$v_1 = \frac{\Delta_1}{\Delta} = \frac{-480}{-18} = 26.667 \text{ V}, \qquad v_3 = \frac{\Delta_3}{\Delta} = \frac{-3120}{-18} = 173.333 \text{ V}$$

$$v_4 = \frac{\Delta_4}{\Delta} = \frac{840}{-18} = -46.667 \text{ V}$$

and $v_2 = v_1 - 20 = 6.667$ V. We have not used Eq. (3.4.5); it can be used to cross check results.

## Practice Problem 3.4

Find $v_1$, $v_2$, and $v_3$ in the circuit in Fig. 3.14 using nodal analysis.

**Answer:** $v_1 = 3.043$ V, $v_2 = -6.956$ V, $v_3 = 0.6522$ V.

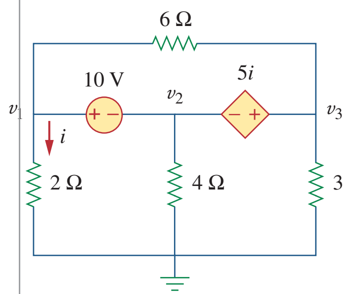


**Figure 3.14**
For Practice Prob. 3.4.

## 3.4 Mesh Analysis

Mesh analysis provides another general procedure for analyzing circuits, using mesh currents as the circuit variables. Using mesh currents instead of element currents as circuit variables is convenient and reduces the number of equations that must be solved simultaneously. Recall that a loop is a closed path with no node passed more than once. A mesh is a loop that does not contain any other loop within it.

Nodal analysis applies KCL to find unknown voltages in a given circuit, while mesh analysis applies KVL to find unknown currents. Mesh analysis is not quite as general as nodal analysis because it is only applicable to a circuit that is *planar*. A planar circuit is one that can be drawn in a plane with no branches crossing one another; otherwise it is *nonplanar*. A circuit may have crossing branches and still be planar if it can be redrawn such that it has no crossing branches. For example, the circuit in Fig. 3.15(a) has two crossing branches, but it can be redrawn as in Fig. 3.15(b). Hence, the circuit in Fig. 3.15(a) is planar. However, the circuit in Fig. 3.16 is nonplanar, because there is no way to redraw it and avoid the branches crossing. Nonplanar circuits can be handled using nodal analysis, but they will not be considered in this text.

Mesh analysis is also known as *loop analysis* or the *mesh-current method.*

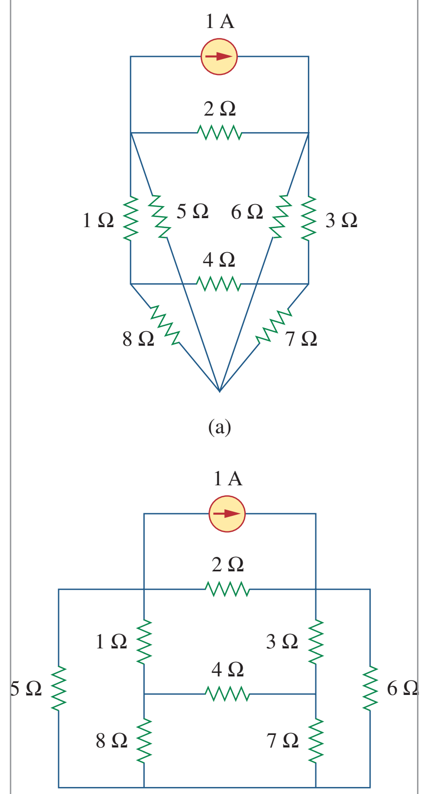


**Figure 3.15**
(a) A planar circuit with crossing branches, (b) the same circuit redrawn with no crossing branches.

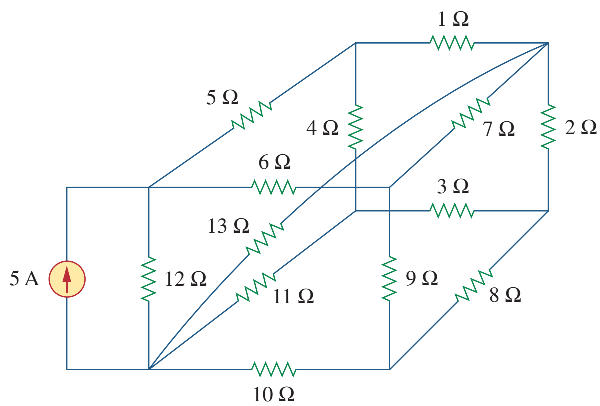


**Figure 3.16**
A nonplanar circuit.

To understand mesh analysis, we should first explain more about what we mean by a mesh.

A **mesh** is a loop which does not contain any other loops within it.

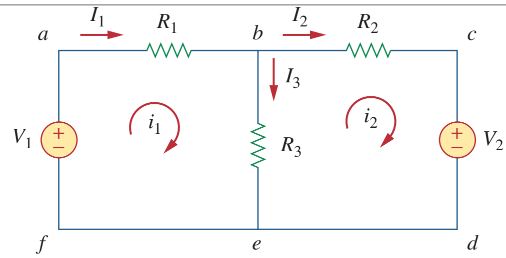


**Figure 3.17**
A circuit with two meshes.

In Fig. 3.17, for example, paths *abefa* and *bcdeb* are meshes, but path *abcdefa* is not a mesh. The current through a mesh is known as *mesh current*. In mesh analysis, we are interested in applying KVL to find the mesh currents in a given circuit.

Although path *abcdefa* is a loop and not a mesh, KVL still holds. This is the reason for loosely using the terms *loop analysis* and *mesh analysis* to mean the same thing.

In this section, we will apply mesh analysis to planar circuits that do not contain current sources. In the next sections, we will consider circuits with current sources. In the mesh analysis of a circuit with $n$ meshes, we take the following three steps.

## Steps to Determine Mesh Currents:

1. Assign mesh currents $i_1, i_2, \ldots, i_n$ to the $n$ meshes.
2. Apply KVL to each of the $n$ meshes. Use Ohm's law to express the voltages in terms of the mesh currents.
3. Solve the resulting $n$ simultaneous equations to get the mesh currents.

The direction of the mesh current is arbitrary—(clockwise or counterclockwise)—and does not affect the validity of the solution.

To illustrate the steps, consider the circuit in Fig. 3.17. The first step requires that mesh currents $i_1$ and $i_2$ are assigned to meshes 1 and 2. Although a mesh current may be assigned to each mesh in an arbitrary direction, it is conventional to assume that each mesh current flows clockwise.

As the second step, we apply KVL to each mesh. Applying KVL to mesh 1, we obtain

$$-V_1 + R_1 i_1 + R_3(i_1 - i_2) = 0$$

or

$$(R_1 + R_3)i_1 - R_3 i_2 = V_1 \tag{3.13}$$

For mesh 2, applying KVL gives

$$R_2 i_2 + V_2 + R_3(i_2 - i_1) = 0$$

or

$$-R_3 i_1 + (R_2 + R_3)i_2 = -V_2 \tag{3.14}$$

Note in Eq. (3.13) that the coefficient of $i_1$ is the sum of the resistances in the first mesh, while the coefficient of $i_2$ is the negative of the resistance common to meshes 1 and 2. Now observe that the same is true in Eq. (3.14). This can serve as a shortcut way of writing the mesh equations. We will exploit this idea in Section 3.6.

The shortcut way will not apply if one mesh current is assumed clockwise and the other assumed anticlockwise, although this is permissible.

The third step is to solve for the mesh currents. Putting Eqs. (3.13) and (3.14) in matrix form yields

$$\begin{bmatrix} R_1 + R_3 & -R_3 \\ -R_3 & R_2 + R_3 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} V_1 \\ -V_2 \end{bmatrix} \tag{3.15}$$

which can be solved to obtain the mesh currents $i_1$ and $i_2$. We are at liberty to use any technique for solving the simultaneous equations. According to Eq. (2.12), if a circuit has $n$ nodes, $b$ branches, and $l$ independent loops or meshes, then $l = b - n + 1$. Hence, $l$ independent simultaneous equations are required to solve the circuit using mesh analysis.

Notice that the branch currents are different from the mesh currents unless the mesh is isolated. To distinguish between the two types of currents, we use $i$ for a mesh current and $I$ for a branch current. The current elements $I_1$, $I_2$, and $I_3$ are algebraic sums of the mesh currents. It is evident from Fig. 3.17 that

$$I_1 = i_1, \qquad I_2 = i_2, \qquad I_3 = i_1 - i_2 \tag{3.16}$$

## Example 3.5

For the circuit in Fig. 3.18, find the branch currents $I_1$, $I_2$, and $I_3$ using mesh analysis.

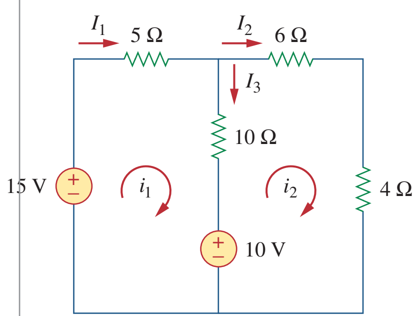


**Figure 3.18**
For Example 3.5.

**Solution:**

We first obtain the mesh currents using KVL. For mesh 1,

$$-15 + 5i_1 + 10(i_1 - i_2) + 10 = 0$$

or

$$3i_1 - 2i_2 = 1$$

For mesh 2,

$$6i_2 + 4i_2 + 10(i_2 - i_1) - 10 = 0$$

or

$$i_1 = 2i_2 - 1 \tag{3.5.2}$$

■ **METHOD 1** Using the substitution method, we substitute Eq. (3.5.2) into Eq. (3.5.1), and write

$$6i_2 - 3 - 2i_2 = 1 \qquad \Rightarrow \qquad i_2 = 1 \text{ A}$$

From Eq. (3.5.2), $i_1 = 2i_2 - 1 = 2 - 1 = 1$ A. Thus,

$$I_1 = i_1 = 1 \text{ A}, \qquad I_2 = i_2 = 1 \text{ A}, \qquad I_3 = i_1 - i_2 = 0$$

■ **METHOD 2** To use Cramer's rule, we cast Eqs. (3.5.1) and (3.5.2) in matrix form as

$$\begin{bmatrix} 3 & -2 \\ -1 & 2 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} 1 \\ 1 \end{bmatrix}$$

We obtain the determinants

$$\Delta = \begin{vmatrix} 3 & -2 \\ -1 & 2 \end{vmatrix} = 6 - 2 = 4$$

$$\Delta_1 = \begin{vmatrix} 1 & -2 \\ 1 & 2 \end{vmatrix} = 2 + 2 = 4, \qquad \Delta_2 = \begin{vmatrix} 3 & 1 \\ -1 & 1 \end{vmatrix} = 3 + 1 = 4$$

Thus,

$$i_1 = \frac{\Delta_1}{\Delta} = 1 \text{ A}, \qquad i_2 = \frac{\Delta_2}{\Delta} = 1 \text{ A}$$

as before.

## Practice Problem 3.5

Calculate the mesh currents $i_1$ and $i_2$ in the circuit of Fig. 3.19.

**Answer:** $i_1 = \frac{2}{3}$ A, $i_2 = 0$ A.

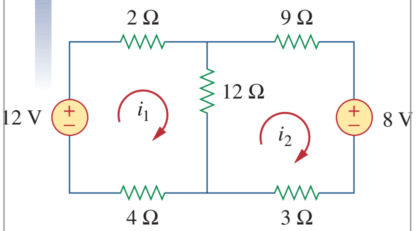


**Figure 3.19**
For Practice Prob. 3.5.

## Example 3.6

Use mesh analysis to find the current $I_o$ in the circuit in Fig. 3.20.

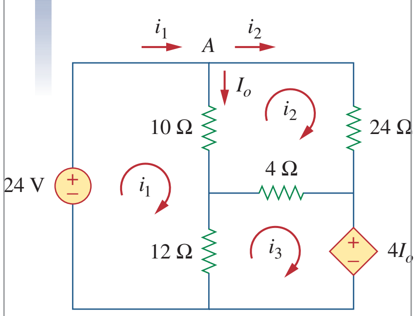


**Figure 3.20**
For Example 3.6.

**Solution:**
We apply KVL to the three meshes in turn. For mesh 1,

$$-24 + 10(i_1 - i_2) + 12(i_1 - i_3) = 0$$

or

$$11i_1 - 5i_2 - 6i_3 = 12 \tag{3.6.1}$$

For mesh 2,

$$24i_2 + 4(i_2 - i_3) + 10(i_2 - i_1) = 0$$

or

$$-5i_1 + 19i_2 - 2i_3 = 0 \tag{3.6.2}$$

For mesh 3,

$$4I_o + 12(i_3 - i_1) + 4(i_3 - i_2) = 0$$

But at node A, $I_o = i_1 - i_2$, so that

$$4(i_1 - i_2) + 12(i_3 - i_1) + 4(i_3 - i_2) = 0$$

or

$$-i_1 - i_2 + 2i_3 = 0 \qquad \textbf{(3.6.3)}$$

In matrix form, Eqs. (3.6.1) to (3.6.3) become

$$\begin{bmatrix} 11 & -5 & -6 \\ -5 & 19 & -2 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \begin{bmatrix} 12 \\ 0 \\ 0 \end{bmatrix}$$

We obtain the determinants as

$$\Delta = \begin{array}{c|ccc|c} & 11 & -5 & -6 & \\ & -5 & 19 & -2 & \\ & -1 & -1 & 2 & \\ - & 11 & -5 & -6 & + \\ - & -5 & 19 & -2 & + \\ - & & & & + \end{array}$$

$$= 418 - 30 - 10 - 114 - 22 - 50 = 192$$

$$\Delta_1 = \begin{array}{c|ccc|c} & 12 & -5 & -6 & \\ & 0 & 19 & -2 & \\ & 0 & -1 & 2 & \\ - & 12 & -5 & -6 & + \\ - & 0 & 19 & -2 & + \\ - & & & & + \end{array} = 456 - 24 = 432$$

$$\Delta_2 = \begin{array}{c|ccc|c} & 11 & 12 & -6 & \\ & -5 & 0 & -2 & \\ & -1 & 0 & 2 & \\ - & 11 & 12 & -6 & + \\ - & -5 & 0 & -2 & + \\ - & & & & + \end{array} = 24 + 120 = 144$$

$$\Delta_3 = \begin{array}{c|ccc|c} & 11 & -5 & 12 & \\ & -5 & 19 & 0 & \\ & -1 & -1 & 0 & \\ - & 11 & -5 & 12 & + \\ - & -5 & 19 & 0 & + \\ - & & & & + \end{array} = 60 + 228 = 288$$

We calculate the mesh currents using Cramer's rule as

$$i_1 = \frac{\Delta_1}{\Delta} = \frac{432}{192} = 2.25 \text{ A}, \qquad i_2 = \frac{\Delta_2}{\Delta} = \frac{144}{192} = 0.75 \text{ A}$$

$$i_3 = \frac{\Delta_3}{\Delta} = \frac{288}{192} = 1.5 \text{ A}$$

Thus, $I_o = i_1 - i_2 = 1.5$ A.

## Practice Problem 3.6

Using mesh analysis, find $I_o$ in the circuit in Fig. 3.21.

**Answer:** $-5$ A.

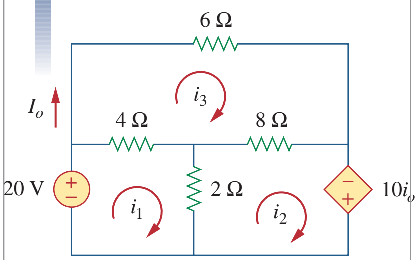


**Figure 3.21**
For Practice Prob. 3.6.

## 3.5 Mesh Analysis with Current Sources

Applying mesh analysis to circuits containing current sources (dependent or independent) may appear complicated. But it is actually much easier than what we encountered in the previous section, because the presence of the current sources reduces the number of equations. Consider the following two possible cases.

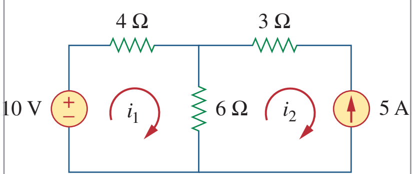


**Figure 3.22**
A circuit with a current source.

■ **CASE 1** When a current source exists only in one mesh: Consider the circuit in Fig. 3.22, for example. We set $i_2 = -5$ A and write a mesh equation for the other mesh in the usual way, that is,

$$-10 + 4i_1 + 6(i_1 - i_2) = 0 \quad \Rightarrow \quad i_1 = -2 \text{ A} \tag{3.17}$$

■ **CASE 2** When a current source exists between two meshes: Consider the circuit in Fig. 3.23(a), for example. We create a *supermesh* by excluding the current source and any elements connected in series with it, as shown in Fig. 3.23(b). Thus,

> A **supermesh** results when two meshes have a (dependent or independent) current source in common.

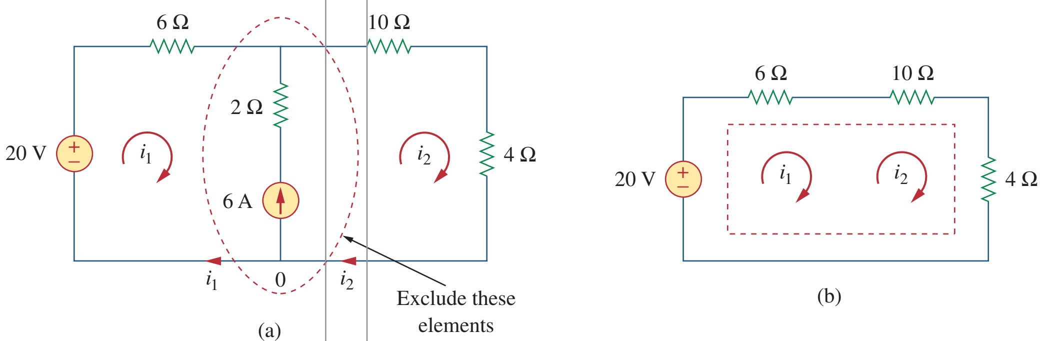


**Figure 3.23**
(a) Two meshes having a current source in common, (b) a supermesh, created by excluding the current source.

As shown in Fig. 3.23(b), we create a supermesh as the periphery of the two meshes and treat it differently. (If a circuit has two or more supermeshes that intersect, they should be combined to form a larger supermesh.) Why treat the supermesh differently? Because mesh analysis applies KVL—which requires that we know the voltage across each branch—and we do not know the voltage across a current source in advance. However, a supermesh must satisfy KVL like any other mesh. Therefore, applying KVL to the supermesh in Fig. 3.23(b) gives

$$-20 + 6i_1 + 10i_2 + 4i_2 = 0$$

or

$$6i_1 + 14i_2 = 20 \tag{3.18}$$

We apply KCL to a node in the branch where the two meshes intersect. Applying KCL to node 0 in Fig. 3.23(a) gives

$$i_2 = i_1 + 6 \tag{3.19}$$

Solving Eqs. (3.18) and (3.19), we get

$$i_1 = -3.2 \text{ A}, \qquad i_2 = 2.8 \text{ A} \tag{3.20}$$

Note the following properties of a supermesh:

1. The current source in the supermesh provides the constraint equation necessary to solve for the mesh currents.
2. A supermesh has no current of its own.
3. A supermesh requires the application of both KVL and KCL.

## Example 3.7

For the circuit in Fig. 3.24, find $i_1$ to $i_4$ using mesh analysis.

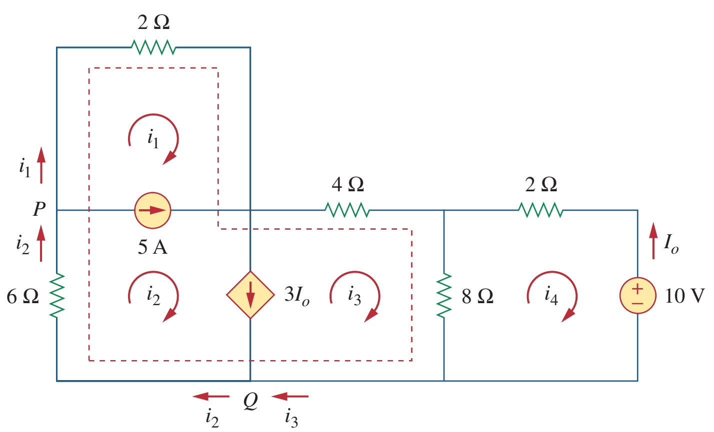


**Figure 3.24**
For Example 3.7.

**Solution:**

Note that meshes 1 and 2 form a supermesh since they have an independent current source in common. Also, meshes 2 and 3 form another supermesh because they have a dependent current source in common. The two supermeshes intersect and form a larger supermesh as shown. Applying KVL to the larger supermesh,

$$2i_1 + 4i_3 + 8(i_3 - i_4) + 6i_2 = 0$$

or

$$i_1 + 3i_2 + 6i_3 - 4i_4 = 0 \tag{3.7.1}$$

For the independent current source, we apply KCL to node $P$:

$$i_2 = i_1 + 5 \tag{3.7.2}$$

For the dependent current source, we apply KCL to node $Q$:

$$i_2 = i_3 + 3i_o$$

But $i_o = -i_4$, hence,

$$i_2 = i_3 - 3i_4 \tag{3.7.3}$$

Applying KVL in mesh 4,

$$2i_4 + 8(i_4 - i_3) + 10 = 0$$

or

$$5i_4 - 4i_3 = -5 \tag{3.7.4}$$

From Eqs. (3.7.1) to (3.7.4),

$$i_1 = -7.5 \text{ A}, \quad i_2 = -2.5 \text{ A}, \quad i_3 = 3.93 \text{ A}, \quad i_4 = 2.143 \text{ A}$$

## Practice Problem 3.7

Use mesh analysis to determine $i_1$, $i_2$, and $i_3$ in Fig. 3.25.

**Answer:** $i_1 = 3.474$ A, $i_2 = 0.4737$ A, $i_3 = 1.1052$ A.

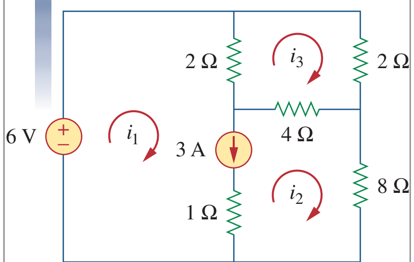


**Figure 3.25**
For Practice Prob. 3.7.

## 3.6 †Nodal and Mesh Analyses by Inspection

This section presents a generalized procedure for nodal or mesh analysis. It is a shortcut approach based on mere inspection of a circuit.

When all sources in a circuit are independent current sources, we do not need to apply KCL to each node to obtain the node-voltage equations as we did in Section 3.2. We can obtain the equations by mere inspection of the circuit. As an example, let us reexamine the circuit in Fig. 3.2, shown again in Fig. 3.26(a) for convenience. The circuit has two nonreference nodes and the node equations were derived in Section 3.2 as

$$\begin{bmatrix} G_1 + G_2 & -G_2 \\ -G_2 & G_2 + G_3 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} I_1 - I_2 \\ I_2 \end{bmatrix} \tag{3.21}$$

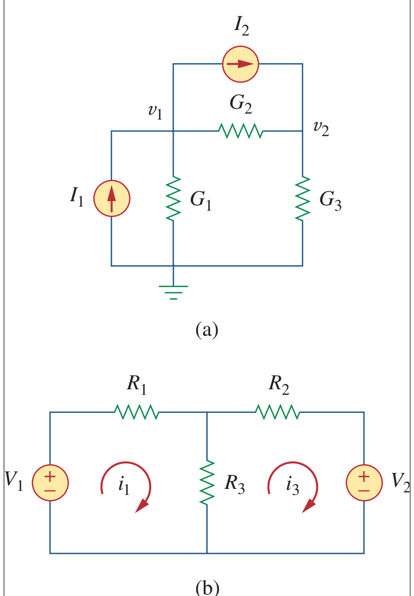


**Figure 3.26**
(a) The circuit in Fig. 3.2, (b) the circuit in Fig. 3.17.

Observe that each of the diagonal terms is the sum of the conductances connected directly to node 1 or 2, while the off-diagonal terms are the negatives of the conductances connected between the nodes. Also, each term on the right-hand side of Eq. (3.21) is the algebraic sum of the currents entering the node.

In general, if a circuit with independent current sources has $N$ nonreference nodes, the node-voltage equations can be written in terms of the conductances as

$$\begin{bmatrix} G_{11} & G_{12} & \dots & G_{1N} \\ G_{21} & G_{22} & \dots & G_{2N} \\ \vdots & \vdots & \vdots & \vdots \\ G_{N1} & G_{N2} & \dots & G_{NN} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_N \end{bmatrix} = \begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_N \end{bmatrix} \tag{3.22}$$

or simply

$$\mathbf{G}\mathbf{v} = \mathbf{i} \tag{3.23}$$

where

$G_{kk}$ = Sum of the conductances connected to node $k$

$G_{kj} = G_{jk}$ = Negative of the sum of the conductances directly connecting nodes $k$ and $j$, $k \neq j$

$v_k$ = Unknown voltage at node $k$

$i_k$ = Sum of all independent current sources directly connected to node $k$, with currents entering the node treated as positive

**G** is called the *conductance matrix*; **v** is the output vector; and **i** is the input vector. Equation (3.22) can be solved to obtain the unknown node voltages. Keep in mind that this is valid for circuits with only independent current sources and linear resistors.

Similarly, we can obtain mesh-current equations by inspection when a linear resistive circuit has only independent voltage sources. Consider the circuit in Fig. 3.17, shown again in Fig. 3.26(b) for convenience. The circuit has two nonreference nodes and the node equations were derived in Section 3.4 as

$$\begin{bmatrix} R_1 + R_3 & -R_3 \\ -R_3 & R_2 + R_3 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} v_1 \\ -v_2 \end{bmatrix} \tag{3.24}$$

We notice that each of the diagonal terms is the sum of the resistances in the related mesh, while each of the off-diagonal terms is the negative of the resistance common to meshes 1 and 2. Each term on the right-hand side of Eq. (3.24) is the algebraic sum taken clockwise of all independent voltage sources in the related mesh.

In general, if the circuit has $N$ meshes, the mesh-current equations can be expressed in terms of the resistances as

$$\begin{bmatrix} R_{11} & R_{12} & \dots & R_{1N} \\ R_{21} & R_{22} & \dots & R_{2N} \\ \vdots & \vdots & \vdots & \vdots \\ R_{N1} & R_{N2} & \dots & R_{NN} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_N \end{bmatrix} = \begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_N \end{bmatrix} \tag{3.25}$$

or simply

$$\mathbf{R}\mathbf{i} = \mathbf{v} \tag{3.26}$$

where

$R_{kk}$ = Sum of the resistances in mesh $k$

$R_{kj} = R_{jk}$ = Negative of the sum of the resistances in common with meshes $k$ and $j$, $k \neq j$

$i_k$ = Unknown mesh current for mesh $k$ in the clockwise direction

$v_k$ = Sum taken clockwise of all independent voltage sources in mesh $k$, with voltage rise treated as positive

**R** is called the *resistance matrix*; **i** is the output vector; and **v** is the input vector. We can solve Eq. (3.25) to obtain the unknown mesh currents.

## Example 3.8

Write the node-voltage matrix equations for the circuit in Fig. 3.27 by inspection.

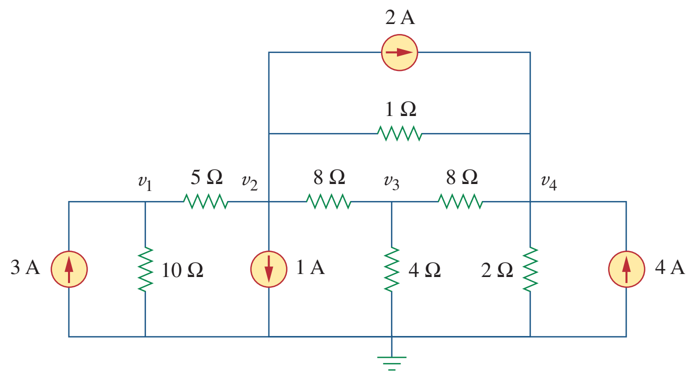


**Figure 3.27**
For Example 3.8.

**Solution:**

The circuit in Fig. 3.27 has four nonreference nodes, so we need four node equations. This implies that the size of the conductance matrix **G**, is 4 by 4. The diagonal terms of **G**, in siemens, are

$$G_{11} = \frac{1}{5} + \frac{1}{10} = 0.3, \qquad G_{22} = \frac{1}{5} + \frac{1}{8} + \frac{1}{1} = 1.325$$

$$G_{33} = \frac{1}{8} + \frac{1}{8} + \frac{1}{4} = 0.5, \qquad G_{44} = \frac{1}{8} + \frac{1}{2} + \frac{1}{1} = 1.625$$

The off-diagonal terms are

$$G_{12} = -\frac{1}{5} = -0.2, \qquad G_{13} = G_{14} = 0$$

$$G_{21} = -0.2, \qquad G_{23} = -\frac{1}{8} = -0.125, \qquad G_{24} = -\frac{1}{1} = -1$$

$$G_{31} = 0, \qquad G_{32} = -0.125, \qquad G_{34} = -\frac{1}{8} = -0.125$$

$$G_{41} = 0, \qquad G_{42} = -1, \qquad G_{43} = -0.125$$

The input current vector **i** has the following terms, in amperes:

$$i_1 = 3, \qquad i_2 = -1 - 2 = -3, \qquad i_3 = 0, \qquad i_4 = 2 + 4 = 6$$

Thus the node-voltage equations are

$$\begin{bmatrix} 0.3 & -0.2 & 0 & 0 \\ -0.2 & 1.325 & -0.125 & -1 \\ 0 & -0.125 & 0.5 & -0.125 \\ 0 & -1 & -0.125 & 1.625 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} = \begin{bmatrix} 3 \\ -3 \\ 0 \\ 6 \end{bmatrix}$$

which can be solved using *MATLAB* to obtain the node voltages $v_1$, $v_2$, $v_3$, and $v_4$.

## Practice Problem 3.8

By inspection, obtain the node-voltage equations for the circuit in Fig. 3.28.

**Answer:**

$$\begin{bmatrix} 1.3 & -0.2 & -1 & 0 \\ -0.2 & 0.2 & 0 & 0 \\ -1 & 0 & 1.25 & -0.25 \\ 0 & 0 & -0.25 & 0.75 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} = \begin{bmatrix} 0 \\ 3 \\ -1 \\ 3 \end{bmatrix}$$

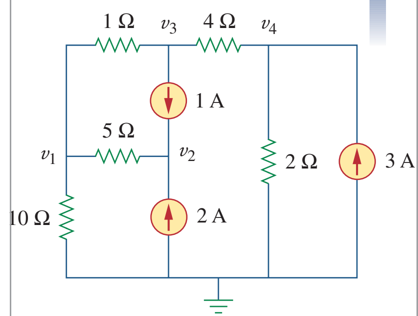


**Figure 3.28**
For Practice Prob. 3.8.

## Example 3.9

By inspection, write the mesh-current equations for the circuit in Fig. 3.29.

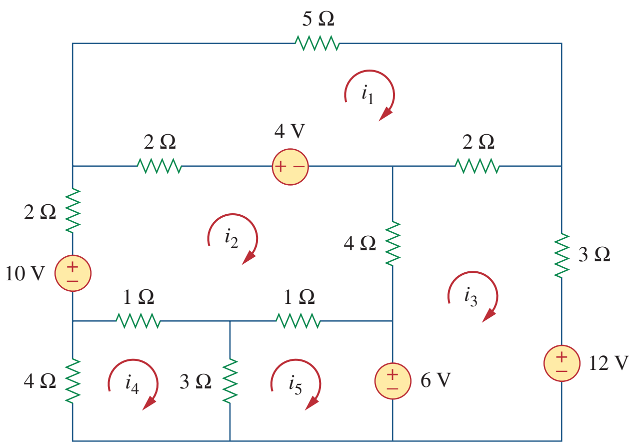


**Figure 3.29**
For Example 3.9.

**Solution:**

We have five meshes, so the resistance matrix is 5 by 5. The diagonal terms, in ohms, are:

$$R_{11} = 5 + 2 + 2 = 9, \quad R_{22} = 2 + 4 + 1 + 1 + 2 = 10$$
$$R_{33} = 2 + 3 + 4 = 9, \quad R_{44} = 1 + 3 + 4 = 8, \quad R_{55} = 1 + 3 = 4$$

The off-diagonal terms are:

$$R_{12} = -2, \quad R_{13} = -2, \quad R_{14} = 0 = R_{15}$$
$$R_{21} = -2, \quad R_{23} = -4, \quad R_{24} = -1, \quad R_{25} = -1$$
$$R_{31} = -2, \quad R_{32} = -4, \quad R_{34} = 0 = R_{35}$$
$$R_{41} = 0, \quad R_{42} = -1, \quad R_{43} = 0, \quad R_{45} = -3$$
$$R_{51} = 0, \quad R_{52} = -1, \quad R_{53} = 0, \quad R_{54} = -3$$

The input voltage vector **v** has the following terms in volts:

$$v_1 = 4, \quad v_2 = 10 - 4 = 6$$
$$v_3 = -12 + 6 = -6, \quad v_4 = 0, \quad v_5 = -6$$

Thus the mesh-current equations are:

$$\begin{bmatrix} 9 & -2 & -2 & 0 & 0 \\ -2 & 10 & -4 & -1 & -1 \\ -2 & -4 & 9 & 0 & 0 \\ 0 & -1 & 0 & 8 & -3 \\ 0 & -1 & 0 & -3 & 4 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \\ i_5 \end{bmatrix} = \begin{bmatrix} 4 \\ 6 \\ -6 \\ 0 \\ -6 \end{bmatrix}$$

From this, we can use *MATLAB* to obtain mesh currents $i_1$, $i_2$, $i_3$, $i_4$, and $i_5$.

## Practice Problem 3.9

By inspection, obtain the mesh-current equations for the circuit in Fig. 3.30.

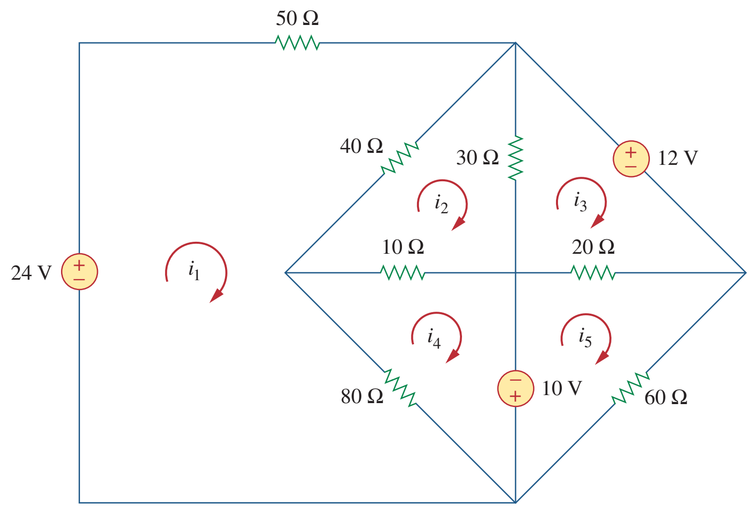


**Figure 3.30**
For Practice Prob. 3.9.

**Answer:**

$$\begin{bmatrix} 170 & -40 & 0 & -80 & 0 \\ -40 & 80 & -30 & -10 & 0 \\ 0 & -30 & 50 & 0 & -20 \\ -80 & -10 & 0 & 90 & 0 \\ 0 & 0 & -20 & 0 & 80 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \\ i_5 \end{bmatrix} = \begin{bmatrix} 24 \\ 0 \\ -12 \\ 10 \\ -10 \end{bmatrix}$$

## 3.7 Nodal Versus Mesh Analysis

Both nodal and mesh analyses provide a systematic way of analyzing a complex network. Someone may ask: Given a network to be analyzed, how do we know which method is better or more efficient? The choice of the better method is dictated by two factors.

The first factor is the nature of the particular network. Networks that contain many series-connected elements, voltage sources, or supermeshes are more suitable for mesh analysis, whereas networks with parallel-connected elements, current sources, or supernodes are more suitable for nodal analysis. Also, a circuit with fewer nodes than meshes is better analyzed using nodal analysis, while a circuit with fewer meshes than nodes is better analyzed using mesh analysis. The key is to select the method that results in the smaller number of equations.

The second factor is the information required. If node voltages are required, it may be expedient to apply nodal analysis. If branch or mesh currents are required, it may be better to use mesh analysis.

It is helpful to be familiar with both methods of analysis, for at least two reasons. First, one method can be used to check the results from the other method, if possible. Second, since each method has its limitations, only one method may be suitable for a particular problem. For example, mesh analysis is the only method to use in analyzing transistor circuits, as we shall see in Section 3.9. But mesh analysis cannot easily be used to solve an op amp circuit, as we shall see in Chapter 5, because there is no direct way to obtain the voltage across the op amp itself. For nonplanar networks, nodal analysis is the only option, because mesh analysis only applies to planar networks. Also, nodal analysis is more amenable to solution by computer, as it is easy to program. This allows one to analyze complicated circuits that defy hand calculation. A computer software package based on nodal analysis is introduced next.

## 3.8 Circuit Analysis with *PSpice*

*PSpice* is a computer software circuit analysis program that we will gradually learn to use throughout the course of this text. This section illustrates how to use *PSpice for Windows* to analyze the dc circuits we have studied so far.

Appendix D provides a tutorial on using *PSpice for Windows*.

The reader is expected to review Sections D.1 through D.3 of Appendix D before proceeding in this section. It should be noted that *PSpice* is only helpful in determining branch voltages and currents when the numerical values of all the circuit components are known.

### Example 3.10

Use *PSpice* to find the node voltages in the circuit of Fig. 3.31.

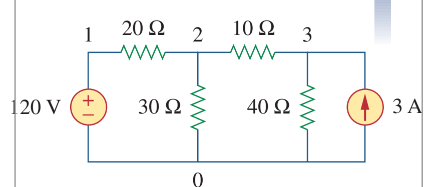


**Figure 3.31**
For Example 3.10.

**Solution:**

The first step is to draw the given circuit using Schematics. If one follows the instructions given in Appendix sections D.2 and D.3, the schematic in Fig. 3.32 is produced. Since this is a dc analysis, we use voltage source VDC and current source IDC. The pseudocomponent VIEWPOINTS are added to display the required node voltages. Once the circuit is drawn and saved as *exam310.sch*, we run *PSpice* by selecting **Analysis/Simulate**. The circuit is simulated and the results

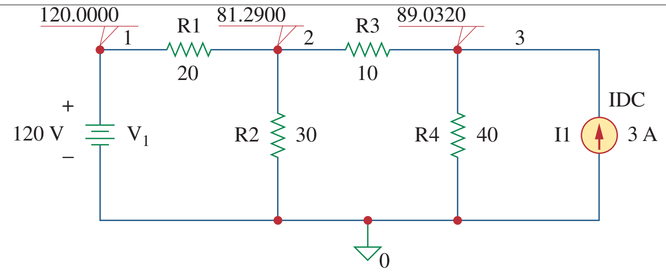


**Figure 3.32**
For Example 3.10; the schematic of the circuit in Fig. 3.31.

are displayed on VIEWPOINTS and also saved in output file *exam310.out*. The output file includes the following:

| NODE | VOLTAGE | NODE | VOLTAGE | NODE | VOLTAGE |
|---|---|---|---|---|---|
| (1) | 120.0000 | (2) | 81.2900 | (3) | 89.0320 |

indicating that $V_1 = 120$ V, $V_2 = 81.29$ V, $V_3 = 89.032$ V.

## Practice Problem 3.10

For the circuit in Fig. 3.33, use *PSpice* to find the node voltages.

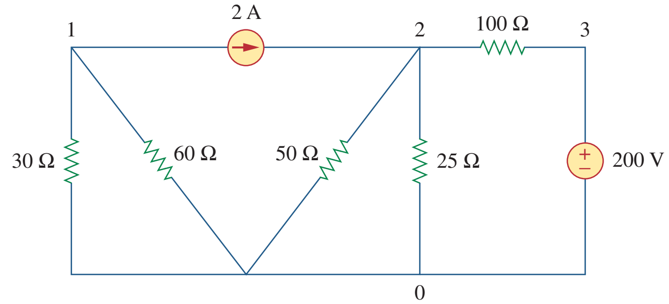


**Figure 3.33**
For Practice Prob. 3.10.

**Answer:** $V_1 = -40$ V, $V_2 = 57.14$ V, $V_3 = 200$ V.

## Example 3.11

In the circuit in Fig. 3.34, determine the currents $i_1$, $i_2$, and $i_3$.

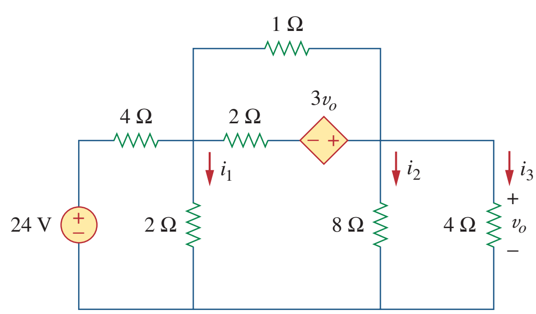


**Figure 3.34**
For Example 3.11.

**Solution:**
The schematic is shown in Fig. 3.35. (The schematic in Fig. 3.35 includes the output results, implying that it is the schematic displayed on the screen *after* the simulation.) Notice that the voltage-controlled voltage source E1 in Fig. 3.35 is connected so that its input is the voltage across the 4-Ω resistor; its gain is set equal to 3. In order to display the required currents, we insert pseudocomponent IPROBES in the appropriate branches. The schematic is saved as *exam311.sch* and simulated by selecting **Analysis/Simulate**. The results are displayed on IPROBES as shown in Fig. 3.35 and saved in output file *exam311.out*. From the output file or the IPROBES, we obtain $i_1 = i_2 = 1.333$ A and $i_3 = 2.667$ A.

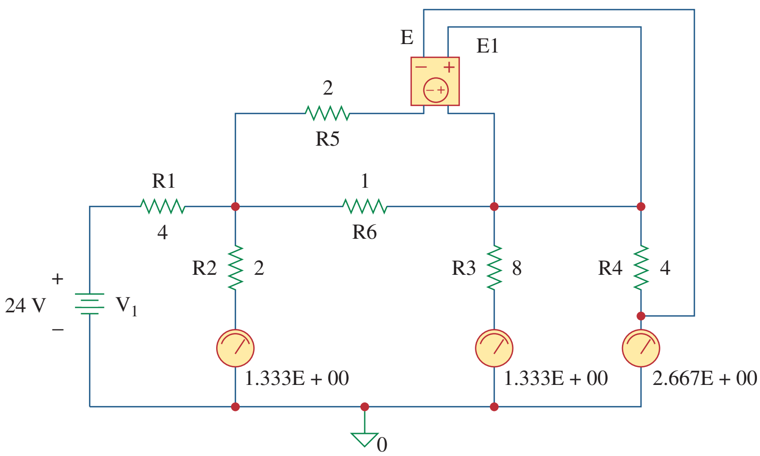


**Figure 3.35**
The schematic of the circuit in Fig. 3.34.

## Practice Problem 3.11

Use *PSpice* to determine currents $i_1$, $i_2$, and $i_3$ in the circuit of Fig. 3.36.

**Answer:** $i_1 = -0.4286$ A, $i_2 = 2.286$ A, $i_3 = 2$ A.

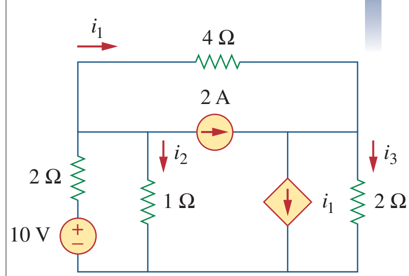


**Figure 3.36**
For Practice Prob. 3.11.

## 3.9 †Applications: DC Transistor Circuits

Most of us deal with electronic products on a routine basis and have some experience with personal computers. A basic component for the integrated circuits found in these electronics and computers is the active, three-terminal device known as the *transistor*. Understanding the transistor is essential before an engineer can start an electronic circuit design.

Figure 3.37 depicts various kinds of transistors commercially available. There are two basic types of transistors: *bipolar junction transistors* (BJTs) and *field-effect transistors* (FETs). Here, we consider only the BJTs, which were the first of the two and are still used today. Our objective is to present enough detail about the BJT to enable us to apply the techniques developed in this chapter to analyze dc transistor circuits.

## Historical Profiles

**William Schockley** (1910–1989), **John Bardeen** (1908–1991), and **Walter Brattain** (1902–1987) co-invented the transistor.

Nothing has had a greater impact on the transition from the "Industrial Age" to the "Age of the Engineer" than the transistor. I am sure that Dr. Shockley, Dr. Bardeen, and Dr. Brattain had no idea they would have this incredible effect on our history. While working at Bell Laboratories, they successfully demonstrated the point-contact transistor, invented by Bardeen and Brattain in 1947, and the junction transistor, which Shockley conceived in 1948 and successfully produced in 1951.

It is interesting to note that the idea of the field-effect transistor, the most commonly used one today, was first conceived in 1925–1928 by J. E. Lilienfeld, a German immigrant to the United States. This is evident from his patents of what appears to be a field-effect transistor. Unfortunately, the technology to realize this device had to wait until 1954 when Shockley's field-effect transistor became a reality. Just think what today would be like if we had this transistor 30 years earlier!

For their contributions to the creation of the transistor, Dr. Shockley, Dr. Bardeen, and Dr. Brattain received, in 1956, the Nobel Prize in physics. It should be noted that Dr. Bardeen is the only individual to win two Nobel prizes in physics; the second came later for work in superconductivity at the University of Illinois.

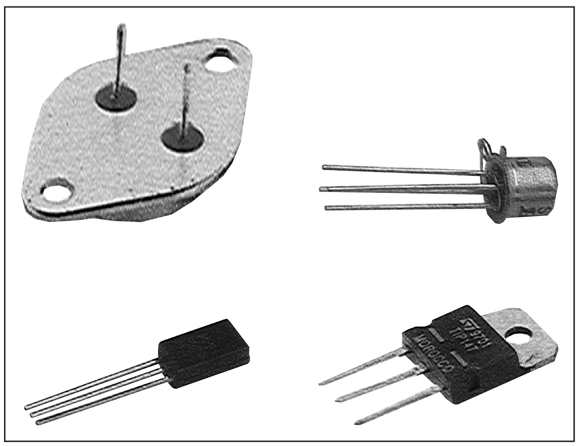

**Figure 3.37**
Various types of transistors.
*(Courtesy of Tech America.)*

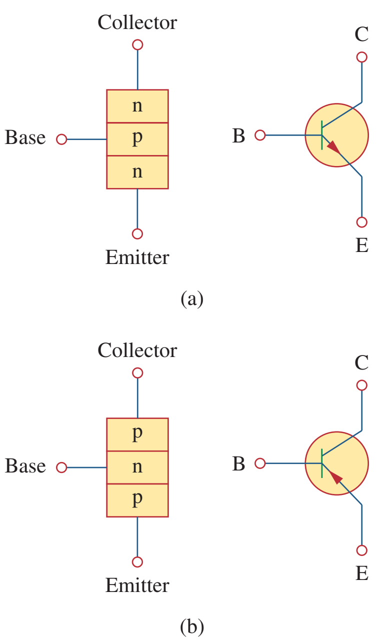


**Figure 3.38**
Two types of BJTs and their circuit symbols: (a) *npn*, (b) *pnp*.

There are two types of BJTs: *npn* and *pnp*, with their circuit symbols as shown in Fig. 3.38. Each type has three terminals, designated as emitter (E), base (B), and collector (C). For the *npn* transistor, the currents and voltages of the transistor are specified as in Fig. 3.39. Applying KCL to Fig. 3.39(a) gives

$$I_E = I_B + I_C \tag{3.27}$$

where $I_E$, $I_C$, and $I_B$ are emitter, collector, and base currents, respectively. Similarly, applying KVL to Fig. 3.39(b) gives

$$V_{CE} + V_{EB} + V_{BC} = 0 \tag{3.28}$$

where $V_{CE}$, $V_{EB}$, and $V_{BC}$ are collector-emitter, emitter-base, and base-collector voltages. The BJT can operate in one of three modes: active, cutoff, and saturation. When transistors operate in the active mode, typically $V_{BE} \simeq 0.7$ V,

$$I_C = \alpha I_E \tag{3.29}$$

where $\alpha$ is called the *common-base current gain*. In Eq. (3.29), $\alpha$ denotes the fraction of electrons injected by the emitter that are collected by the collector. Also,

$$\boxed{I_C = \beta I_B} \tag{3.30}$$

where $\beta$ is known as the *common-emitter current gain*. The $\alpha$ and $\beta$ are characteristic properties of a given transistor and assume constant values for that transistor. Typically, $\alpha$ takes values in the range of 0.98 to 0.999, while $\beta$ takes values in the range 50 to 1000. From Eqs. (3.27) to (3.30), it is evident that

$$I_E = (1 + \beta)I_B \tag{3.31}$$

and

$$\beta = \frac{\alpha}{1 - \alpha} \tag{3.32}$$

These equations show that, in the active mode, the BJT can be modeled as a dependent current-controlled current source. Thus, in circuit analysis, the dc equivalent model in Fig. 3.40(b) may be used to replace the *npn* transistor in Fig. 3.40(a). Since $\beta$ in Eq. (3.32) is large, a small base current controls large currents in the output circuit. Consequently, the bipolar transistor can serve as an amplifier, producing both current gain and voltage gain. Such amplifiers can be used to furnish a considerable amount of power to transducers such as loudspeakers or control motors.

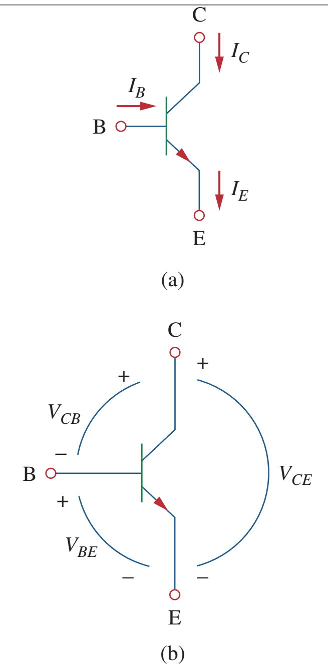


**Figure 3.39**
The terminal variables of an *npn* transistor: (a) currents, (b) voltages.

In fact, transistor circuits provide motivation to study dependent sources.

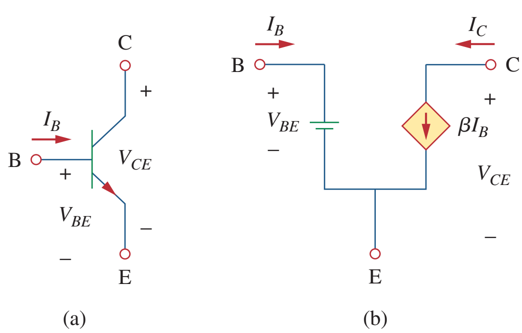


**Figure 3.40**
(a) An *npn* transistor, (b) its dc equivalent model.

It should be observed in the following examples that one cannot directly analyze transistor circuits using nodal analysis because of the potential difference between the terminals of the transistor. Only when the transistor is replaced by its equivalent model can we apply nodal analysis.

## Example 3.12

Find $I_B$, $I_C$, and $v_o$ in the transistor circuit of Fig. 3.41. Assume that the transistor operates in the active mode and that $\beta = 50$.

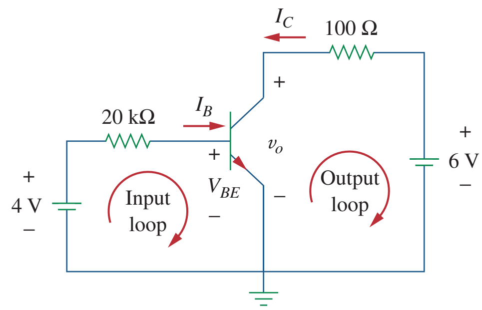


**Figure 3.41**
For Example 3.12.

**Solution:**
For the input loop, KVL gives

$$-4 + I_B(20 \times 10^3) + V_{BE} = 0$$

Since $V_{BE} = 0.7$ V in the active mode,

$$I_B = \frac{4 - 0.7}{20 \times 10^3} = 165\ \mu\text{A}$$

But

$$I_C = \beta I_B = 50 \times 165\ \mu\text{A} = 8.25\ \text{mA}$$

For the output loop, KVL gives

$$-v_o - 100 I_C + 6 = 0$$

or

$$v_o = 6 - 100 I_C = 6 - 0.825 = 5.175\ \text{V}$$

Note that $v_o = V_{CE}$ in this case.

## Practice Problem 3.12

For the transistor circuit in Fig. 3.42, let $\beta = 100$ and $V_{BE} = 0.7$ V. Determine $v_o$ and $V_{CE}$.

**Answer:** 2.876 V, 1.984 V.

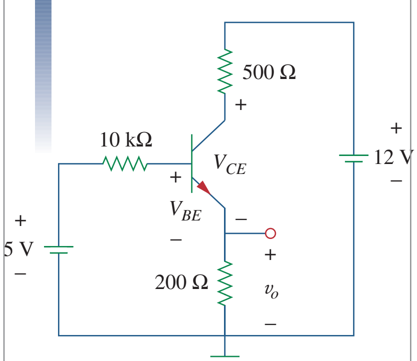


**Figure 3.42**
For Practice Prob. 3.12.

## Example 3.13

For the BJT circuit in Fig. 3.43, $\beta = 150$ and $V_{BE} = 0.7$ V. Find $v_o$.

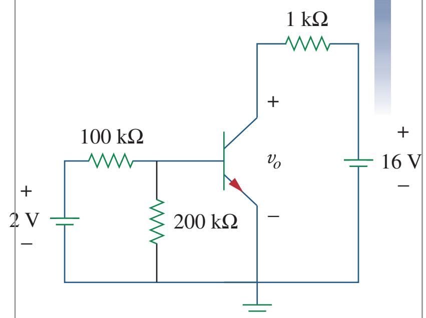


**Figure 3.43**
For Example 3.13.

**Solution:**

1. **Define.** The circuit is clearly defined and the problem is clearly stated. There appear to be no additional questions that need to be asked.
2. **Present.** We are to determine the output voltage of the circuit shown in Fig. 3.43. The circuit contains an ideal transistor with $\beta = 150$ and $V_{BE} = 0.7$ V.
3. **Alternative.** We can use mesh analysis to solve for $v_o$. We can replace the transistor with its equivalent circuit and use nodal analysis. We can try both approaches and use them to check each other. As a third check, we can use the equivalent circuit and solve using *PSpice*.
4. **Attempt**

**METHOD 1** Working with Fig. 3.44(a), we start with the first loop.

$$-2 + 100\text{k}I_1 + 200\text{k}(I_1 - I_2) = 0 \qquad \text{or} \qquad 3I_1 - 2I_2 = 2 \times 10^{-5} \tag{3.13.1}$$

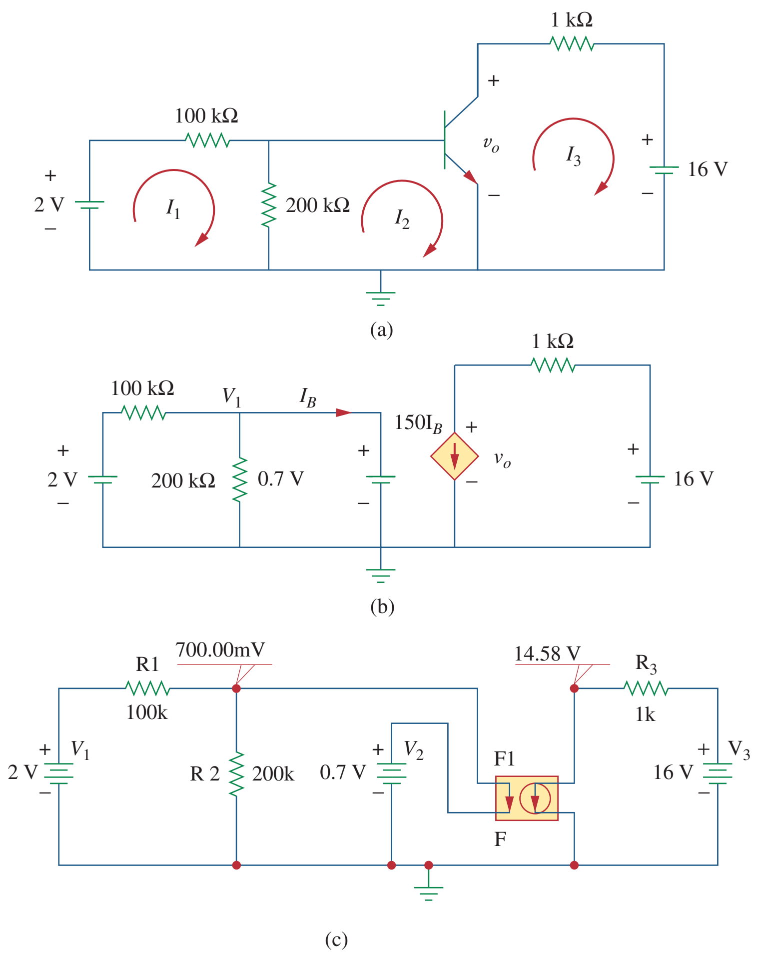


**Figure 3.44**
Solution of the problem in Example 3.13: (a) Method 1, (b) Method 2, (c) Method 3.

Now for loop number 2.

$$200\text{k}(I_2 - I_1) + V_{BE} = 0 \quad \text{or} \quad -2I_1 + 2I_2 = -0.7 \times 10^{-5} \tag{3.13.2}$$

Since we have two equations and two unknowns, we can solve for $I_1$ and $I_2$. Adding Eq. (3.13.1) to (3.13.2) we get;

$$I_1 = 1.3 \times 10^{-5}\text{A} \quad \text{and} \quad I_2 = (-0.7 + 2.6)10^{-5}/2 = 9.5\ \mu\text{A}$$

Since $I_3 = -150I_2 = -1.425$ mA, we can now solve for $v_o$ using loop 3:

$$-v_o + {}^1\text{k}I_3 + 16 = 0 \quad \text{or} \quad v_o = -1.425 + 16 = \underline{\mathbf{14.575\ V}}$$

**METHOD 2** Replacing the transistor with its equivalent circuit produces the circuit shown in Fig. 3.44(b). We can now use nodal analysis to solve for $v_o$.

At node number 1 $V_1 = 0.7$ V:

$$(0.7 - 2)/100\text{k} + 0.7/200\text{k} + I_B = 0 \quad \text{or} \quad I_B = 9.5\ \mu\text{A}$$

At node number 2 we have:

$$150I_B + (v_o - 16)/1\text{k} = 0 \quad \text{or}$$
$$v_o = 16 - 150 \times 10^3 \times 9.5 \times 10^{-6} = \underline{\mathbf{14.575\ V}}$$

5. **Evaluate.** The answers check, but to further check we can use *PSpice* (Method 3), which gives us the solution shown in Fig. 3.44(c).
6. **Satisfactory?** Clearly, we have obtained the desired answer with a very high confidence level. We can now present our work as a solution to the problem.

## Practice Problem 3.13

The transistor circuit in Fig. 3.45 has $\beta = 80$ and $V_{BE} = 0.7$ V. Find $v_o$ and $I_o$.

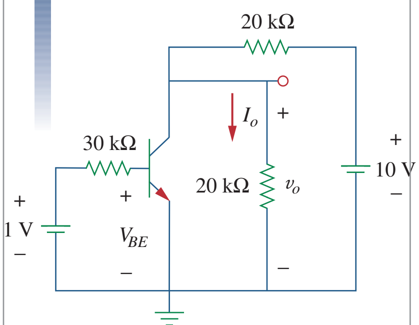


**Figure 3.45**
For Practice Prob. 3.13.

**Answer:** −3 V, −150 $\mu$A.

## 3.10 Summary

1. Nodal analysis is the application of Kirchhoff's current law at the nonreference nodes. (It is applicable to both planar and nonplanar circuits.) We express the result in terms of the node voltages. Solving the simultaneous equations yields the node voltages.
2. A supernode consists of two nonreference nodes connected by a (dependent or independent) voltage source.
3. Mesh analysis is the application of Kirchhoff's voltage law around meshes in a planar circuit. We express the result in terms of mesh currents. Solving the simultaneous equations yields the mesh currents.

4. A supermesh consists of two meshes that have a (dependent or independent) current source in common.
5. Nodal analysis is normally used when a circuit has fewer node equations than mesh equations. Mesh analysis is normally used when a circuit has fewer mesh equations than node equations.
6. Circuit analysis can be carried out using *PSpice*.
7. DC transistor circuits can be analyzed using the techniques covered in this chapter.

## Review Questions

**3.1** At node 1 in the circuit in Fig. 3.46, applying KCL gives:

(a) $2 + \frac{12 - v_1}{3} = \frac{v_1}{6} + \frac{v_1 - v_2}{4}$

(b) $2 + \frac{v_1 - 12}{3} = \frac{v_1}{6} + \frac{v_2 - v_1}{4}$

(c) $2 + \frac{12 - v_1}{3} = \frac{0 - v_1}{6} + \frac{v_1 - v_2}{4}$

(d) $2 + \frac{v_1 - 12}{3} = \frac{0 - v_1}{6} + \frac{v_2 - v_1}{4}$

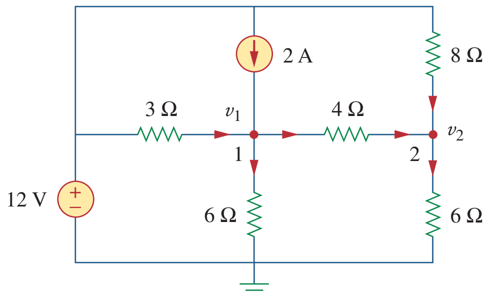


**Figure 3.46**
For Review Questions 3.1 and 3.2.

**3.2** In the circuit in Fig. 3.46, applying KCL at node 2 gives:

(a) $\frac{v_2 - v_1}{4} + \frac{v_2}{8} = \frac{v_2}{6}$

(b) $\frac{v_1 - v_2}{4} + \frac{v_2}{8} = \frac{v_2}{6}$

(c) $\frac{v_1 - v_2}{4} + \frac{12 - v_2}{8} = \frac{v_2}{6}$

(d) $\frac{v_2 - v_1}{4} + \frac{v_2 - 12}{8} = \frac{v_2}{6}$

**3.3** For the circuit in Fig. 3.47, $v_1$ and $v_2$ are related as:

(a) $v_1 = 6i + 8 + v_2$ (b) $v_1 = 6i - 8 + v_2$
(c) $v_1 = -6i + 8 + v_2$ (d) $v_1 = -6i - 8 + v_2$

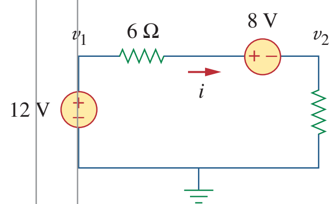


**Figure 3.47**
For Review Questions 3.3 and 3.4.

**3.4** In the circuit in Fig. 3.47, the voltage $v_2$ is:

(a) −8 V (b) −1.6 V
(c) 1.6 V (d) 8 V

**3.5** The current $i$ in the circuit in Fig. 3.48 is:

(a) −2.667 A (b) −0.667 A
(c) 0.667 A (d) 2.667 A

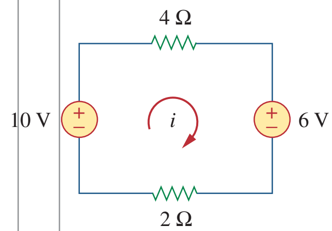


**Figure 3.48**
For Review Questions 3.5 and 3.6.

**3.6** The loop equation for the circuit in Fig. 3.48 is:

(a) $-10 + 4i + 6 + 2i = 0$
(b) $10 + 4i + 6 + 2i = 0$
(c) $10 + 4i - 6 + 2i = 0$
(d) $-10 + 4i - 6 + 2i = 0$

**3.7** In the circuit in Fig. 3.49, current $i_1$ is:

(a) 4 A (b) 3 A (c) 2 A (d) 1 A

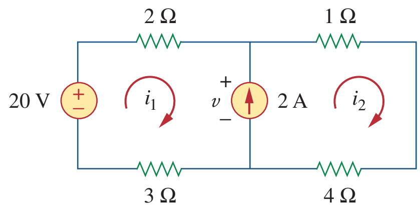


**Figure 3.49**
For Review Questions 3.7 and 3.8.

**3.8** The voltage $v$ across the current source in the circuit of Fig. 3.49 is:

(a) 20 V (b) 15 V (c) 10 V (d) 5 V

**3.9** The *PSpice* part name for a current-controlled voltage source is:

(a) EX (b) FX (c) HX (d) GX

**3.10** Which of the following statements are not true of the pseudocomponent IPROBE:

(a) It must be connected in series.

(b) It plots the branch current.

(c) It displays the current through the branch in which it is connected.

(d) It can be used to display voltage by connecting it in parallel.

(e) It is used only for dc analysis.

(f) It does not correspond to a particular circuit element.

*Answers: 3.1a, 3.2c, 3.3a, 3.4d, 3.5c, 3.6a, 3.7d, 3.8b, 3.9c, 3.10b,d.*

# Problems

## Sections 3.2 and 3.3 Nodal Analysis

**3.1** Determine $I_x$ in the circuit shown in Fig. 3.50 using nodal analysis.

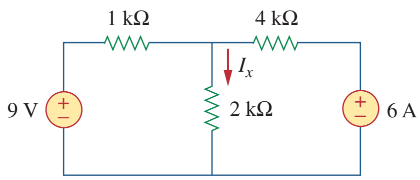


**Figure 3.50**
For Prob. 3.1.

**3.2** For the circuit in Fig. 3.51, obtain $v_1$ and $v_2$.

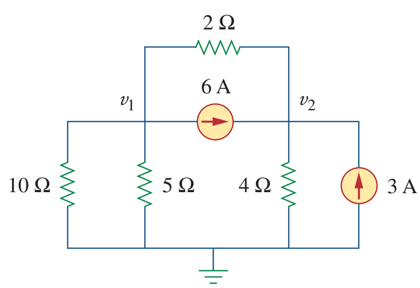


**Figure 3.51**
For Prob. 3.2.

**3.3** Find the currents $I_1$ through $I_4$ and the voltage $v_o$ in the circuit in Fig. 3.52.

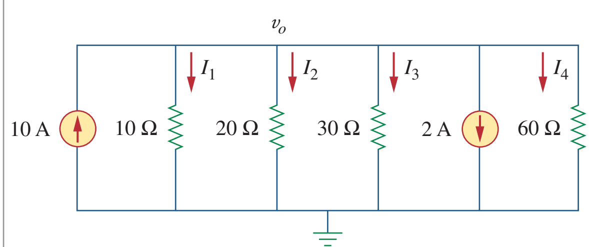


**Figure 3.52**
For Prob. 3.3.

**3.4** Given the circuit in Fig. 3.53, calculate the currents $I_1$ through $I_4$.

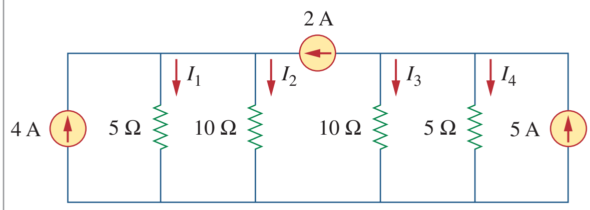


**Figure 3.53**
For Prob. 3.4.

**3.5** Obtain $v_o$ in the circuit of Fig. 3.54.

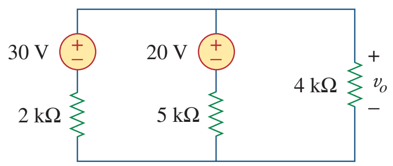


**Figure 3.54**
For Prob. 3.5.

**3.6** Use nodal analysis to obtain $v_o$ in the circuit in Fig. 3.55.

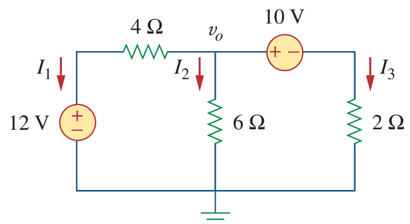


**Figure 3.55**
For Prob. 3.6.

**3.7** Apply nodal analysis to solve for $V_x$ in the circuit in Fig. 3.56.

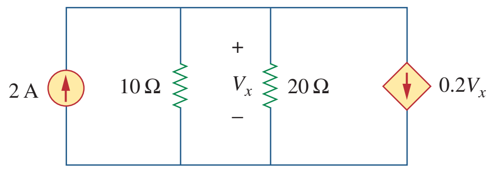


**Figure 3.56**
For Prob. 3.7.

**3.8** Using nodal analysis, find $v_o$ in the circuit of Fig. 3.57.

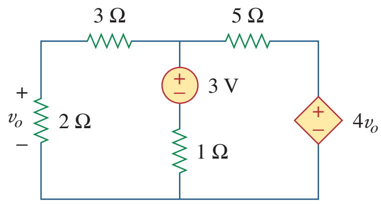


**Figure 3.57**
For Prob. 3.8.

**3.9** Determine $I_b$ in the circuit in Fig. 3.58 using nodal analysis.

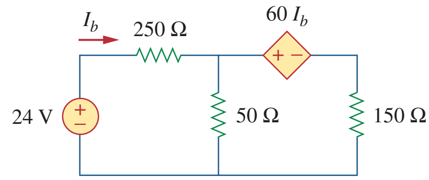


**Figure 3.58**
For Prob. 3.9.

**3.10** Find $I_o$ in the circuit in Fig. 3.59.

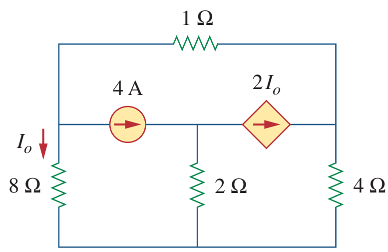


**Figure 3.59**
For Prob. 3.10.

**3.11** Find $V_o$ and the power dissipated in all the resistors in the circuit of Fig. 3.60.

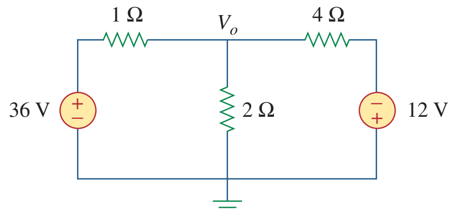


**Figure 3.60**
For Prob. 3.11.

**3.12** Using nodal analysis, determine $V_o$ in the circuit in Fig. 3.61.

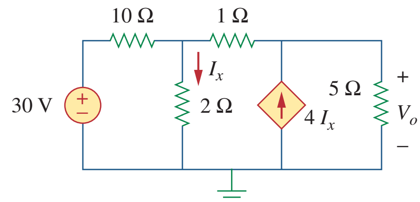


**Figure 3.61**
For Prob. 3.12.

**3.13** Calculate $v_1$ and $v_2$ in the circuit in Fig. 3.62 using nodal analysis.

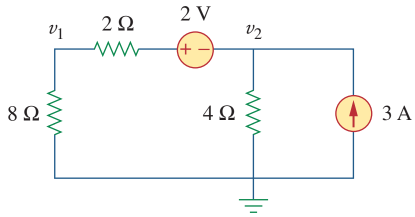


**Figure 3.62**
For Prob. 3.13.

**3.14** Using nodal analysis, find $v_o$ in the circuit of Fig. 3.63.

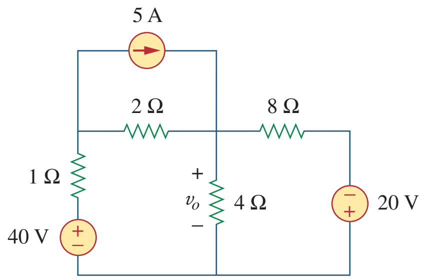


**Figure 3.63**
For Prob. 3.14.

**3.15** Apply nodal analysis to find $i_o$ and the power dissipated in each resistor in the circuit of Fig. 3.64.

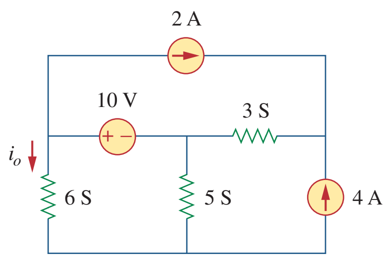


**Figure 3.64**
For Prob. 3.15.

**3.16** Determine voltages $v_1$ through $v_3$ in the circuit of Fig. 3.65 using nodal analysis.

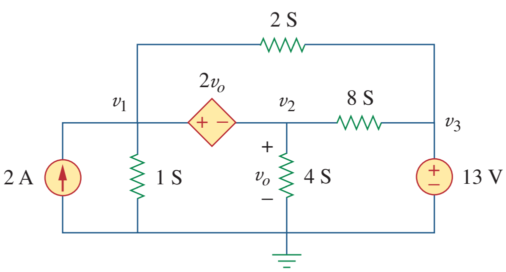


**Figure 3.65**
For Prob. 3.16.

**3.17** Using nodal analysis, find current $i_o$ in the circuit of Fig. 3.66.

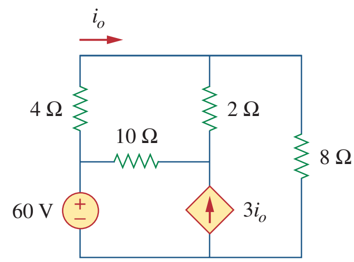


**Figure 3.66**
For Prob. 3.17.

**3.18** Determine the node voltages in the circuit in Fig. 3.67 using nodal analysis.

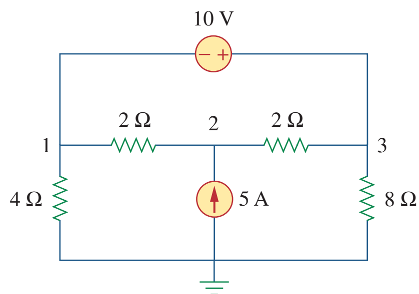


**Figure 3.67**
For Prob. 3.18.

**3.19** Use nodal analysis to find $v_1$, $v_2$, and $v_3$ in the circuit in Fig. 3.68.

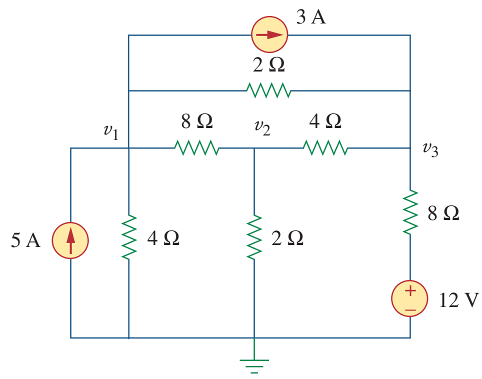


**Figure 3.68**
For Prob. 3.19.

**3.20** For the circuit in Fig. 3.69, find $v_1$, $v_2$, and $v_3$ using nodal analysis.

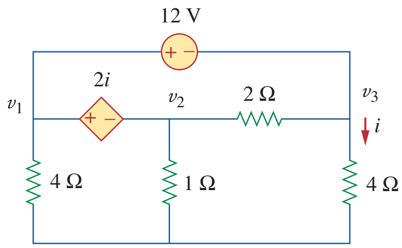


**Figure 3.69**
For Prob. 3.20.

**3.21** For the circuit in Fig. 3.70, find $v_1$ and $v_2$ using nodal analysis.

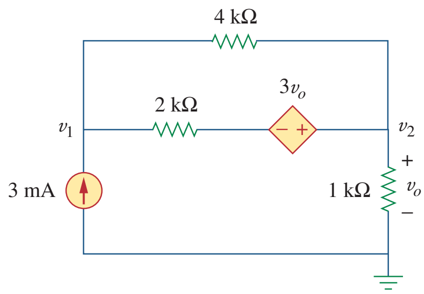


**Figure 3.70**
For Prob. 3.21.

**3.22** Determine $v_1$ and $v_2$ in the circuit in Fig. 3.71.

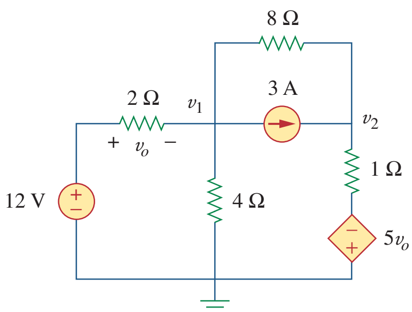


**Figure 3.71**
For Prob. 3.22.

**3.23** Use nodal analysis to find $V_o$ in the circuit of Fig. 3.72.

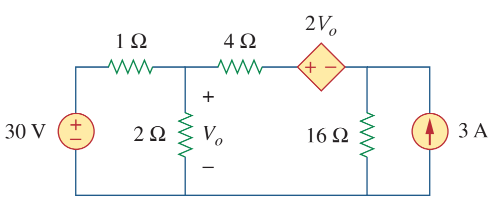


**Figure 3.72**
For Prob. 3.23.

**3.24** Use nodal analysis and *MATLAB* to find $V_o$ in the circuit in Fig. 3.73.

ML

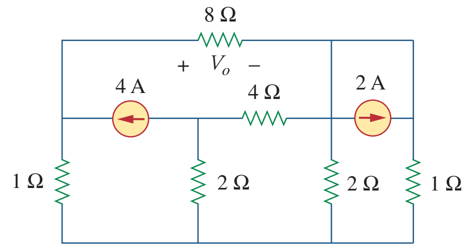


**Figure 3.73**
For Prob. 3.24.

**3.25** Use nodal analysis along with *MATLAB* to determine the node voltages in Fig. 3.74.

ML

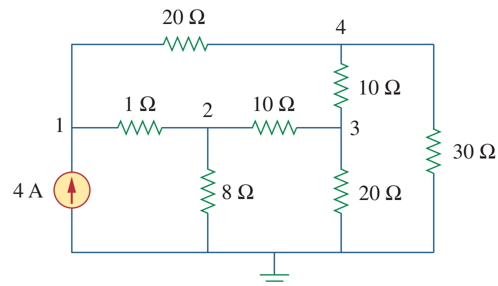


**Figure 3.74**
For Prob. 3.25.

**3.26** Calculate the node voltages $v_1$, $v_2$, and $v_3$ in the circuit of Fig. 3.75.

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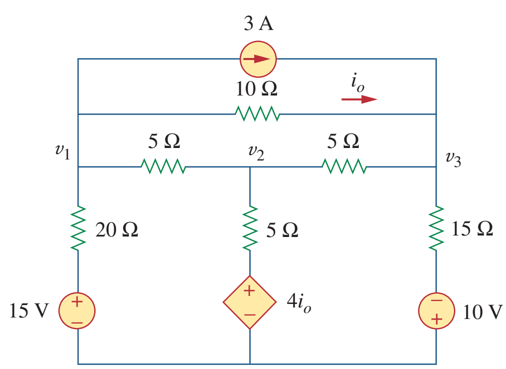



**Figure 3.75**
For Prob. 3.26.

***3.27** Use nodal analysis to determine voltages $v_1$, $v_2$, and $v_3$ in the circuit in Fig. 3.76.

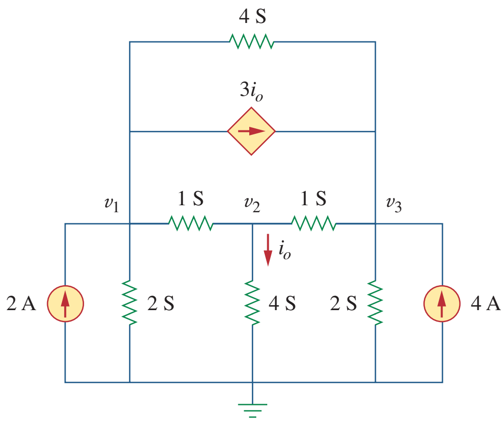



**Figure 3.76**
For Prob. 3.27.

***3.28** Use *MATLAB* to find the voltages at nodes $a$, $b$, $c$, and $d$ in the circuit of Fig. 3.77.

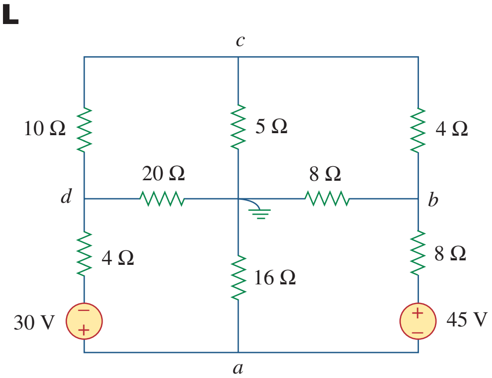



**Figure 3.77**
For Prob. 3.28.

**3.29** Use *MATLAB* to solve for the node voltages in the circuit of Fig. 3.78.

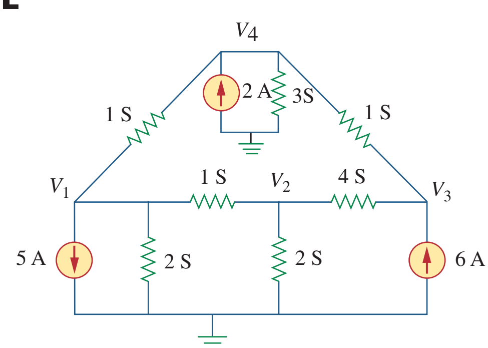



**Figure 3.78**
For Prob. 3.29.

* An asterisk indicates a challenging problem.

**3.30** Using nodal analysis, find $v_o$ and $I_o$ in the circuit of Fig. 3.79.

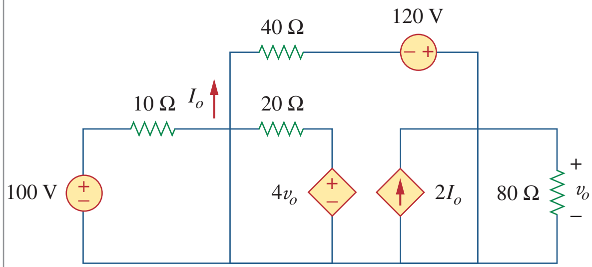



**Figure 3.79**
For Prob. 3.30.

**3.31** Find the node voltages for the circuit in Fig. 3.80.

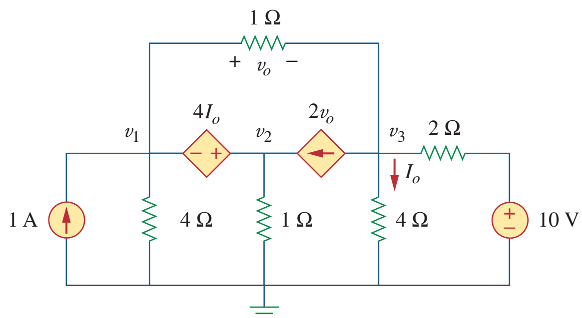



**Figure 3.80**
For Prob. 3.31.

***3.32** Obtain the node voltages $v_1$, $v_2$, and $v_3$ in the circuit of Fig. 3.81.

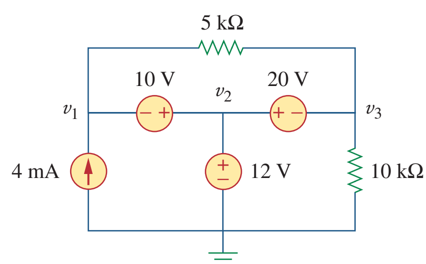
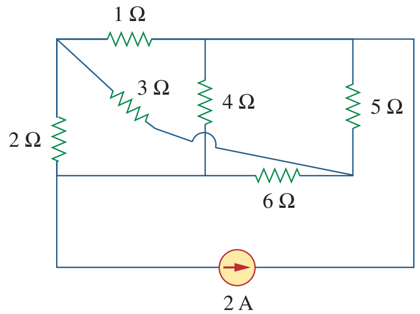


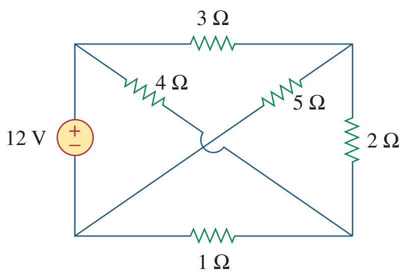

**Figure 3.81**
For Prob. 3.32.

## Sections 3.4 and 3.5 Mesh Analysis

**3.33** Which of the circuits in Fig. 3.82 is planar? For the planar circuit, redraw the circuits with no crossing branches.



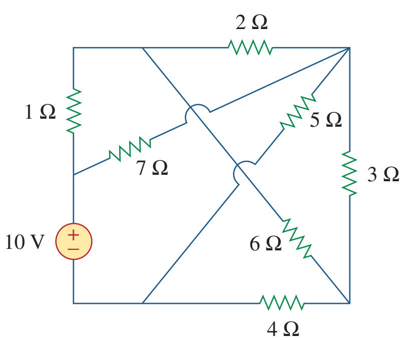

(a)



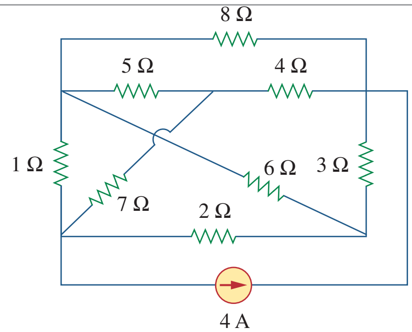

(b)

**Figure 3.82**
For Prob. 3.33.

**3.34** Determine which of the circuits in Fig. 3.83 is planar and redraw it with no crossing branches.




(a)




(b)

**Figure 3.83**
For Prob. 3.34.

**3.35** Rework Prob. 3.5 using mesh analysis.

**3.36** Rework Prob. 3.6 using mesh analysis.

**3.37** Solve Prob. 3.8 using mesh analysis.

**3.38** Apply mesh analysis to the circuit in Fig. 3.84 and obtain $I_o$.

ML

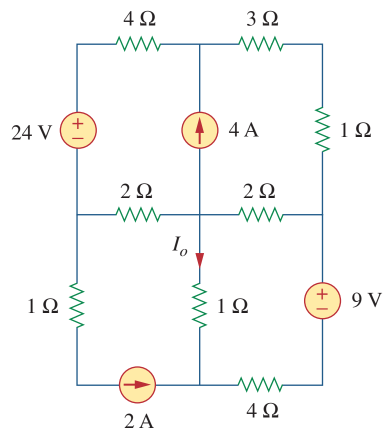



**Figure 3.84**
For Prob. 3.38.

**3.39** Determine the mesh currents $i_1$ and $i_2$ in the circuit shown in Fig. 3.85.

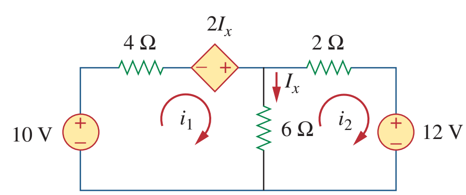



**Figure 3.85**
For Prob. 3.39.

**3.40** For the bridge network in Fig. 3.86, find $i_o$ using mesh analysis.

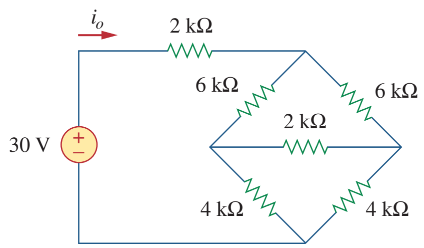



**Figure 3.86**
For Prob. 3.40.

**3.41** Apply mesh analysis to find $i$ in Fig. 3.87.

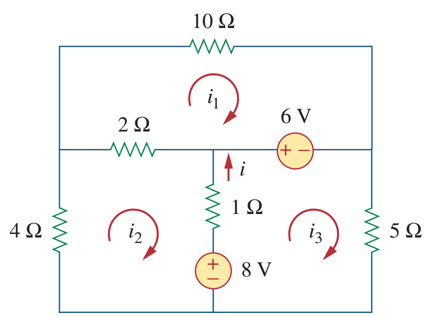



**Figure 3.87**
For Prob. 3.41.

**3.42** Determine the mesh currents in the circuit of Fig. 3.88.

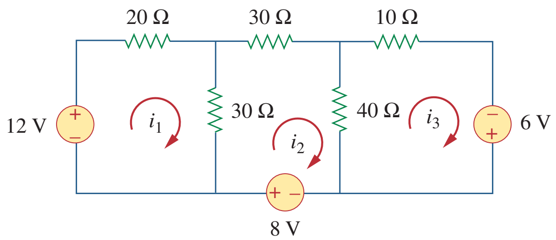



**Figure 3.88**
For Prob. 3.42.

**3.43** Use mesh analysis to find $v_{ab}$ and $i_o$ in the circuit in Fig. 3.89.

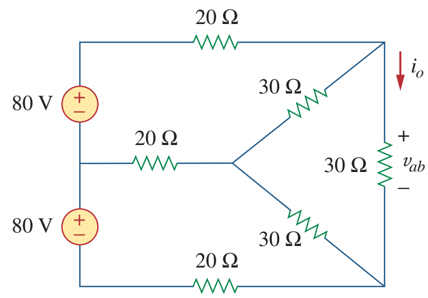



**Figure 3.89**
For Prob. 3.43.

**3.44** Use mesh analysis to obtain $i_o$ in the circuit of Fig. 3.90.

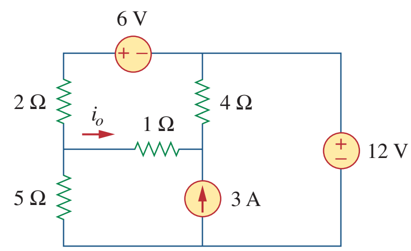



**Figure 3.90**
For Prob. 3.44.

**3.45** Find current $i$ in the circuit in Fig. 3.91.

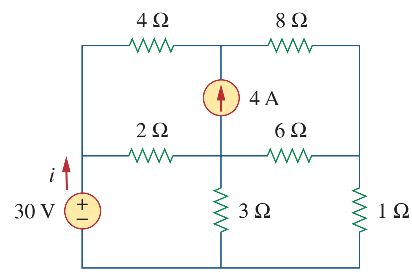



**Figure 3.91**
For Prob. 3.45.

**3.46** Calculate the mesh currents $i_1$ and $i_2$ in Fig. 3.92.

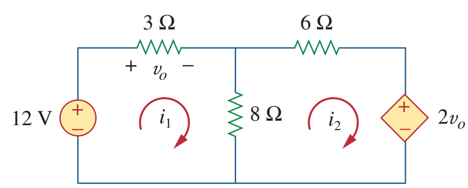



**Figure 3.92**
For Prob. 3.46.

**3.47** Rework Prob. 3.19 using mesh analysis.

**3.48** Determine the current through the 10-kΩ resistor in the circuit in Fig. 3.93 using mesh analysis.

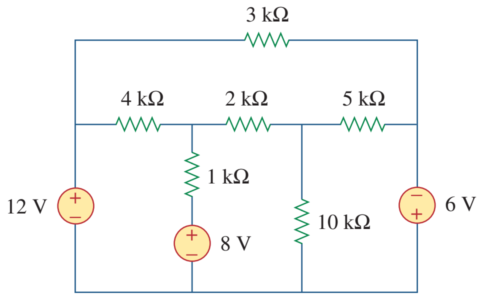



**Figure 3.93**
For Prob. 3.48.

**3.49** Find $v_o$ and $i_o$ in the circuit of Fig. 3.94.

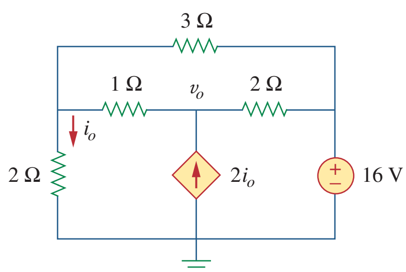



**Figure 3.94**
For Prob. 3.49.

**3.50** Use mesh analysis to find the current $i_o$ in the circuit in Fig. 3.95.

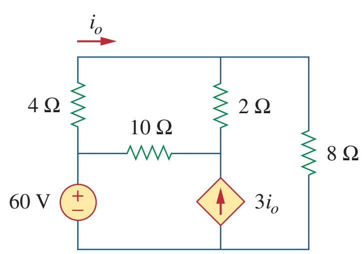



**Figure 3.95**
For Prob. 3.50.

**3.51** Apply mesh analysis to find $v_o$ in the circuit in Fig. 3.96.

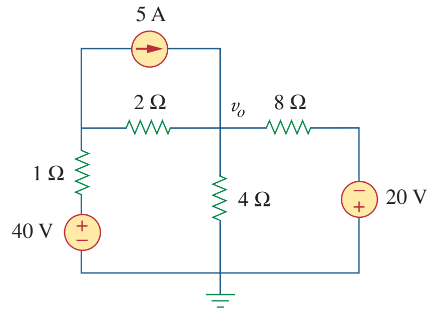



**Figure 3.96**
For Prob. 3.51.

**3.52** Use mesh analysis to find $i_1$, $i_2$, and $i_3$ in the circuit of Fig. 3.97.

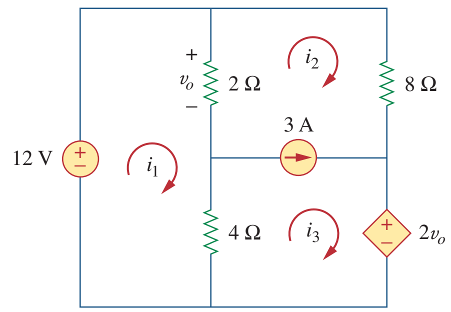



**Figure 3.97**
For Prob. 3.52.

**3.53** Find the mesh currents in the circuit of Fig. 3.98 using *MATLAB*.

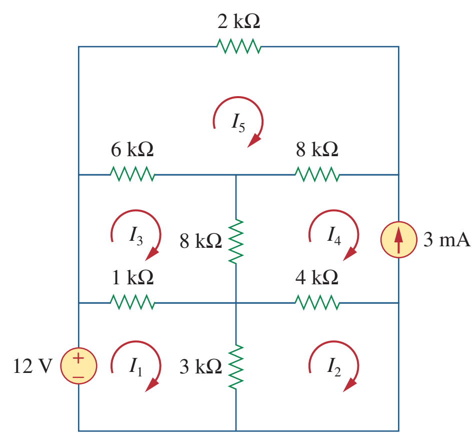



**Figure 3.98**
For Prob. 3.53.

**3.54** Find the mesh currents $i_1$, $i_2$, and $i_3$ in the circuit in Fig. 3.99.

ML

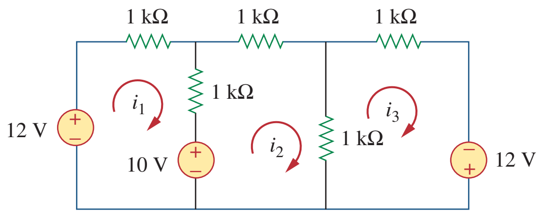



**Figure 3.99**
For Prob. 3.54.

***3.55** In the circuit of Fig. 3.100, solve for $I_1$, $I_2$, and $I_3$.

ML

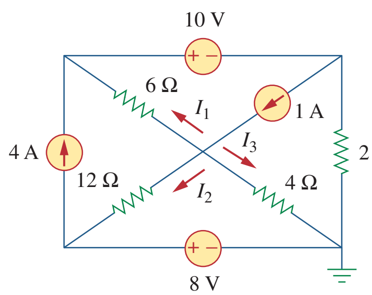



**Figure 3.100**
For Prob. 3.55.

**3.56** Determine $v_1$ and $v_2$ in the circuit of Fig. 3.101.

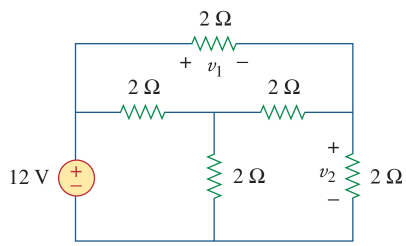



**Figure 3.101**
For Prob. 3.56.

**3.57** In the circuit in Fig. 3.102, find the values of $R$, $V_1$, and $V_2$ given that $i_o = 18$ mA.

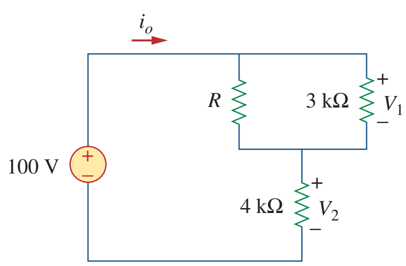



**Figure 3.102**
For Prob. 3.57.

**3.58** Find $i_1$, $i_2$, and $i_3$ in the circuit in Fig. 3.103.

ML

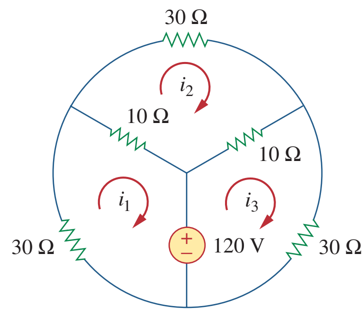



**Figure 3.103**
For Prob. 3.58.

**3.59** Rework Prob. 3.30 using mesh analysis.

ML

**3.60** Calculate the power dissipated in each resistor in the circuit in Fig. 3.104.

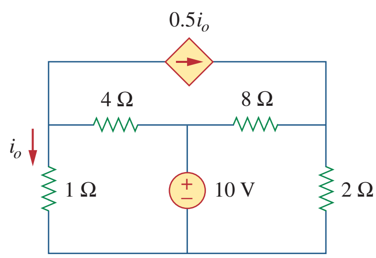



**Figure 3.104**
For Prob. 3.60.

**3.61** Calculate the current gain $i_o/i_s$ in the circuit of Fig. 3.105.

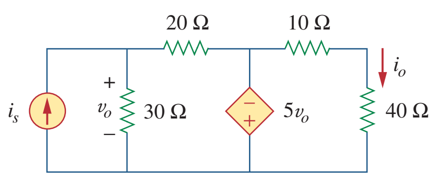



**Figure 3.105**
For Prob. 3.61.

**3.62** Find the mesh currents $i_1$, $i_2$, and $i_3$ in the network of Fig. 3.106.

ML

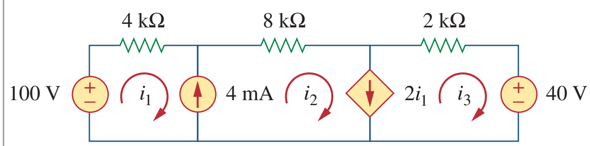



**Figure 3.106**
For Prob. 3.62.

**3.63** Find $v_x$ and $i_x$ in the circuit shown in Fig. 3.107.

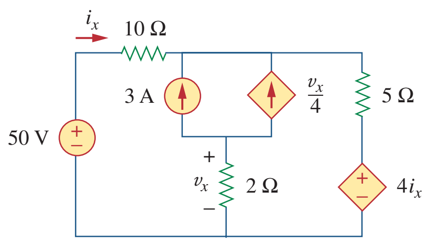



**Figure 3.107**
For Prob. 3.63.

**3.64** Find $v_o$ and $i_o$ in the circuit of Fig. 3.108.

ML ps

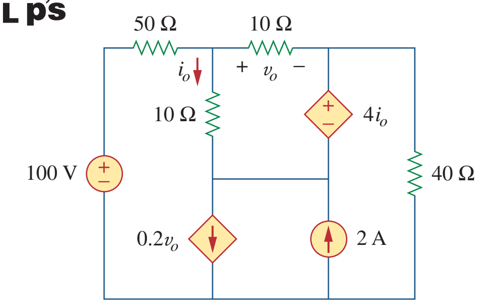



**Figure 3.108**
For Prob. 3.64.

**3.65** Use *MATLAB* to solve for the mesh currents in the circuit of Fig. 3.109.

ML

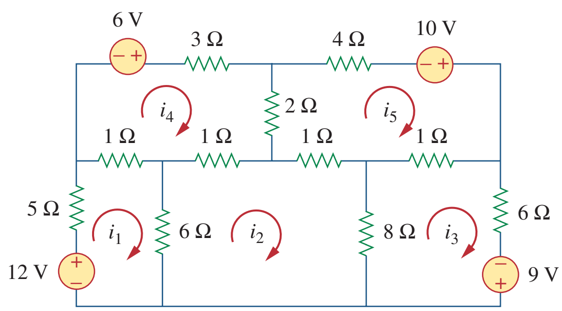



**Figure 3.109**
For Prob. 3.65.

**3.66** Write a set of mesh equations for the circuit in Fig. 3.110. Use *MATLAB* to determine the mesh currents.

ML

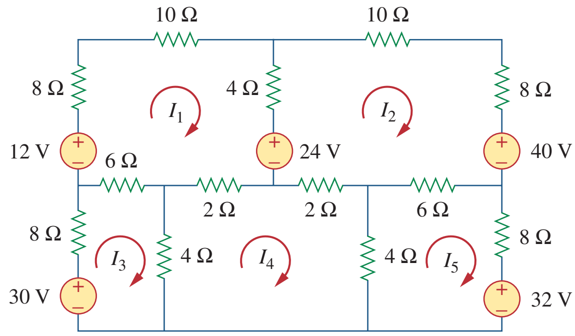



**Figure 3.110**
For Prob. 3.66.

## Section 3.6 Nodal and Mesh Analyses by Inspection

**3.67** Obtain the node-voltage equations for the circuit in Fig. 3.111 by inspection. Then solve for $V_o$.

ML

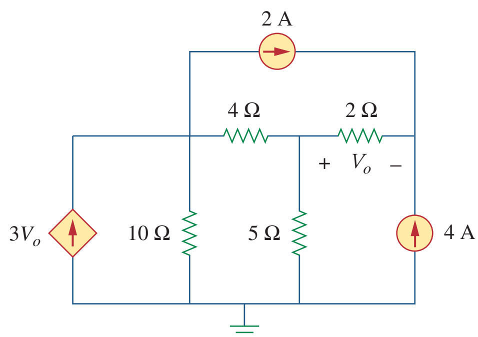



**Figure 3.111**
For Prob. 3.67.

**3.68** Find the voltage $V_o$ in the circuit of Fig. 3.112.

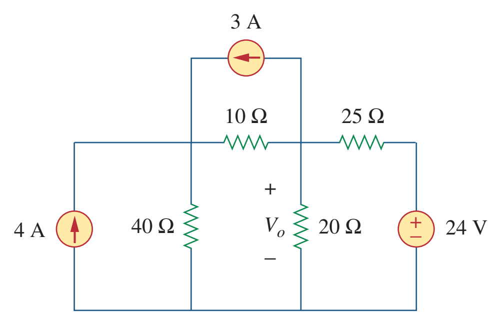



**Figure 3.112**
For Prob. 3.68.

**3.69** For the circuit shown in Fig. 3.113, write the node-voltage equations by inspection.

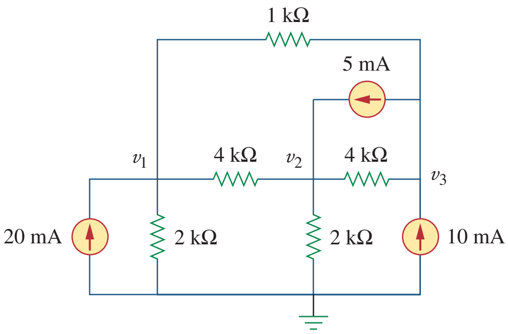



**Figure 3.113**
For Prob. 3.69.

**3.70** Write the node-voltage equations by inspection and then determine values of $V_1$ and $V_2$ in the circuit in Fig. 3.114.

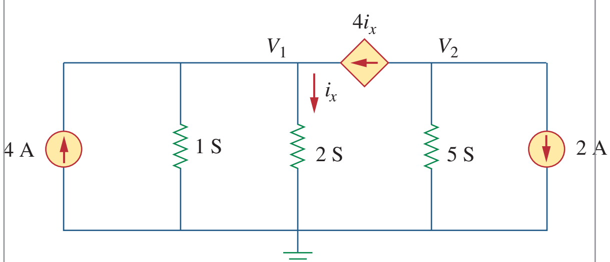



**Figure 3.114**
For Prob. 3.70.

**3.71** Write the mesh-current equations for the circuit in Fig. 3.115. Next, determine the values of $I_1$, $I_2$, and $I_3$.

ML

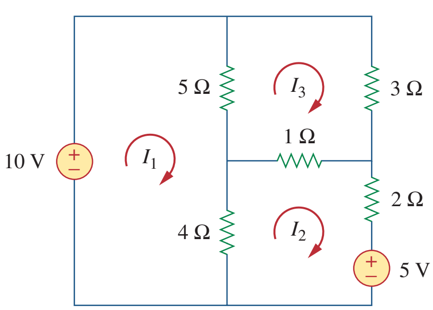



**Figure 3.115**
For Prob. 3.71.

**3.72** By inspection, write the mesh-current equations for the circuit in Fig. 3.116.

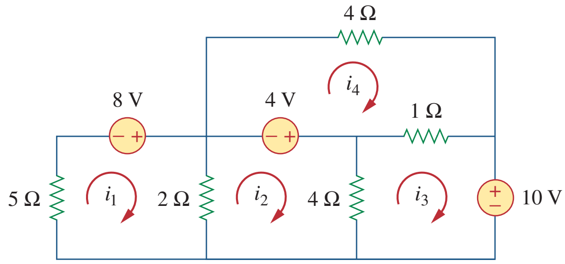



**Figure 3.116**
For Prob. 3.72.

**3.73** Write the mesh-current equations for the circuit in Fig. 3.117.

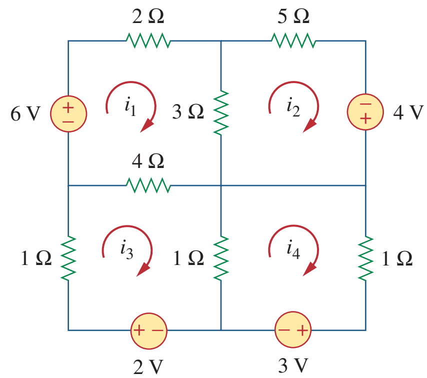



**Figure 3.117**
For Prob. 3.73.

**3.74** By inspection, obtain the mesh-current equations for the circuit in Fig. 3.118.

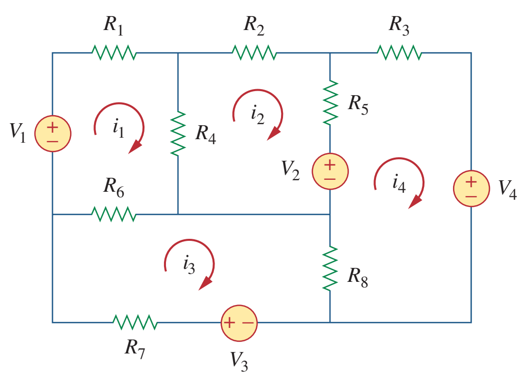



**Figure 3.118**
For Prob. 3.74.

## Section 3.8 Circuit Analysis with *PSpice*

**3.75** Use *PSpice* to solve Prob. 3.58.

**3.76** Use *PSpice* to solve Prob. 3.27.

**3.77** Solve for $V_1$ and $V_2$ in the circuit of Fig. 3.119 using *PSpice*.

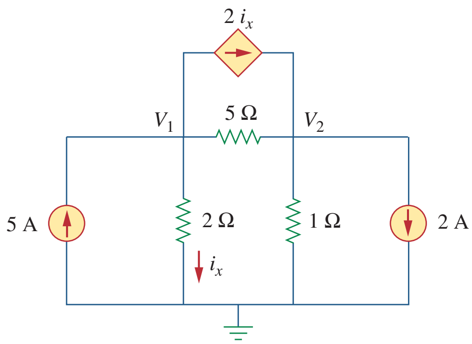



**Figure 3.119**
For Prob. 3.77.

**3.78** Solve Prob. 3.20 using *PSpice*.

**3.79** Rework Prob. 3.28 using *PSpice*.

**3.80** Find the nodal voltages $v_1$ through $v_4$ in the circuit in Fig. 3.120 using *PSpice*.

ML

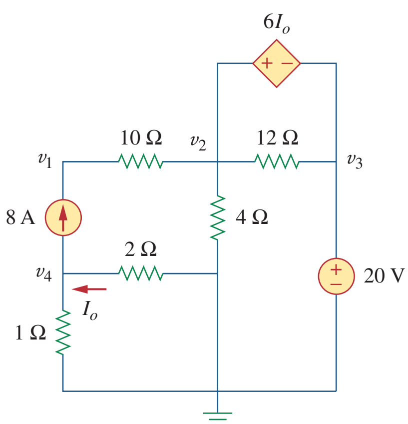



**Figure 3.120**
For Prob. 3.80.

**3.81** Use *PSpice* to solve the problem in Example 3.4.

**3.82** If the Schematics Netlist for a network is as follows, draw the network.

```
R_R1    1   2   2K
R_R2    2   0   4K
R_R3    3   0   8K
R_R4    3   4   6K
R_R5    1   3   3K
V_VS    4   0   DC      100
I_IS    0   1   DC      4
F_F1    1   3   VF_F1   2
VF_F1   5   0   0V
E_E1    3   2   1       3     3
```

**3.83** The following program is the Schematics Netlist of a particular circuit. Draw the circuit and determine the voltage at node 2.

```
R_R1   1   2   20
R_R2   2   0   50
R_R3   2   3   70
R_R4   3   0   30
V_VS   1   0   20V
I_IS   2   0   DC    2A
```

## Section 3.9 Applications

**3.84** Calculate $v_o$ and $I_o$ in the circuit of Fig. 3.121.

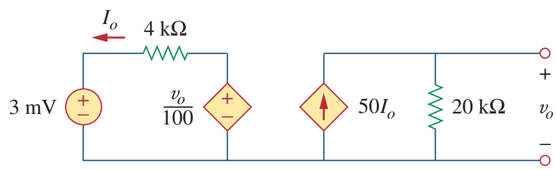



**Figure 3.121**
For Prob. 3.84.

**3.85** An audio amplifier with a resistance of 9 Ω supplies power to a speaker. What should be the resistance of the speaker for maximum power to be delivered?

**3.86** For the simplified transistor circuit of Fig. 3.122, calculate the voltage $v_o$.

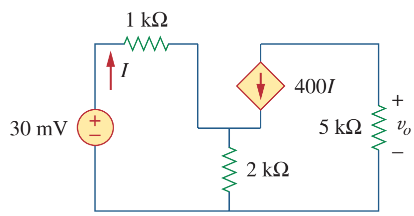



**Figure 3.122**
For Prob. 3.86.

**3.87** For the circuit in Fig. 3.123, find the gain $v_o/v_s$.

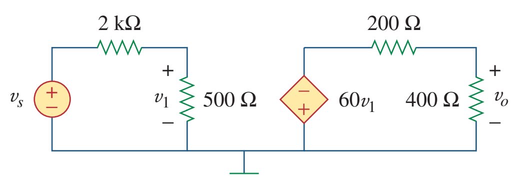



**Figure 3.123**
For Prob. 3.87.

***3.88** Determine the gain $v_o/v_s$ of the transistor amplifier circuit in Fig. 3.124.

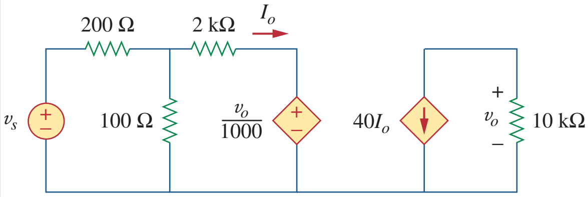



**Figure 3.124**
For Prob. 3.88.

**3.89** For the transistor circuit shown in Fig. 3.125, find $I_B$ and $V_{CE}$. Let $\beta = 100$, and $V_{BE} = 0.7$ V.

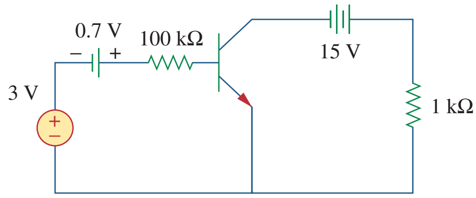



**Figure 3.125**
For Prob. 3.89.

**3.90** Calculate $v_s$ for the transistor in Fig. 3.126 given that $v_o = 4$ V, $\beta = 150$, $V_{BE} = 0.7$ V.

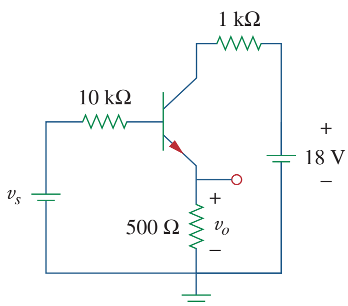



**Figure 3.126**
For Prob. 3.90.

## Comprehensive Problem

***3.93** Rework Example 3.11 with hand calculation.

**3.91** For the transistor circuit of Fig. 3.127, find $I_B$, $V_{CE}$, and $v_o$. Take $\beta = 200$, $V_{BE} = 0.7$ V.

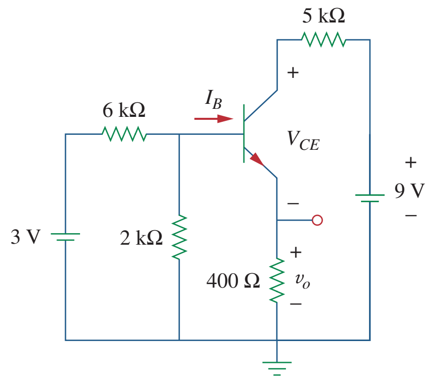



**Figure 3.127**
For Prob. 3.91.

**3.92** Find $I_B$ and $V_C$ for the circuit in Fig. 3.128. Let $\beta = 100$, $V_{BE} = 0.7$ V.

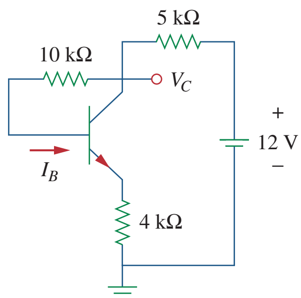



**Figure 3.128**
For Prob. 3.92.