Mixed-Signal Front End Set-Top Box, Cable Modem

AD9879

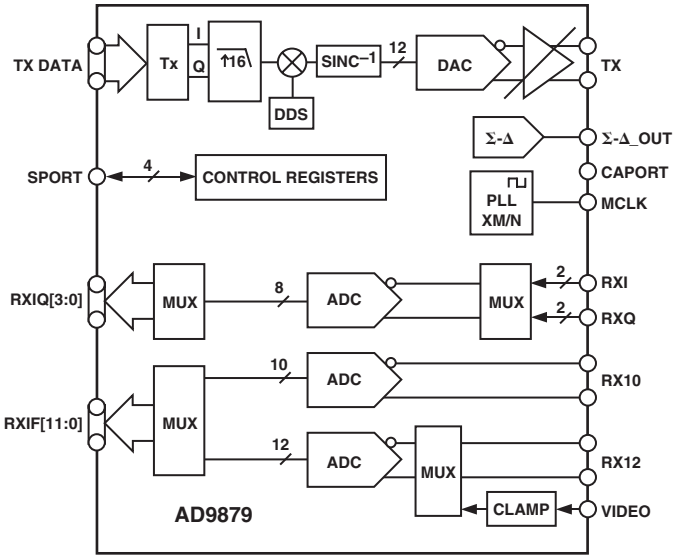
FEATURES

Low Cost 3.3 V MxFE™ for
DOCSIS EURO DOCSIS DVB DAVIC Compliant
Set-Top Box and Cable Modem Applications
232 MHz Quadrature Digital Upconverter
12-Bit Direct IF DAC (TxDAC+™)
Up to 65 MHz Carrier Frequency DDS
Programmable Sampling Clock Rates
16× Upsampling Interpolation LPF
Single-Tone Frequency Synthesis
Analog Tx Output Level Adjust
Direct Cable Amp Interface
12-Bit, 33 MSPS Direct IF ADC
with Optional Video Clamping Input
10-Bit, 33 MSPS Direct IF ADC
Dual 7-Bit, 16.5 MSPS Sampling I/Q ADC
12-Bit Sigma-Delta Auxiliary DAC

APPLICATIONS

Cable Modem and Satellite Systems
Set-Top Boxes
Power Line Modem
PC Multimedia
Digital Communications
Data and Video Modems
QAM, OFDM, FSK Modulation

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9879 is a single-supply cable modem/set-top box mixed signal front end. The device contains a transmit path interpolation filter, a complete quadrature digital upconverter, and a transmit DAC. The receive path contains a 12-bit ADC, a 10-bit ADC, and dual 7-Bit ADCs. All internally required clocks and an output system clock are generated by the PLL from a single crystal or clock input.

The transmit path interpolation filter provides an upsampling factor of 16× with an output signal bandwidth as high as 8.3 MHz. Carrier frequencies up to 65 MHz with 26 bits of frequency tuning resolution can be generated by the direct digital synthesizer (DDS). The transmit DAC resolution is 12 bits and can run at sampling rates as high as 232 MSPS. Analog output scaling from 0 dB to 7.5 dB in 0.5 dB steps is available to preserve SNR when reduced output levels are required.

The 12-bit and 10-bit IF ADCs can convert direct IF inputs up to 70 MHz and run at sample rates up to 33 MSPS. A video input with an adjustable signal clamping level, along with the 10-bit ADC, allow the AD9879 to process an NTSC and a QAM channel simultaneously.

The programmable sigma-delta DAC can be used to control external components, such as variable gain amplifiers (VGAs) or voltage controlled tuners. The CA PORT provides an interface to the AD8321/AD8323 or AD8322/AD8327 programmable gain amplifier (PGA) cable drivers enabling host processor control via the MxFE SPORT. The AD9879 is available in a 100-lead MQFP package. It offers enhanced receive path undersampling performance and lower cost when compared with the pin compatible AD9873. The AD9879 is specified over the commercial (–40°C to +85°C) temperature range.

REV. 0

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AD9879–SPECIFICATIONS (V_{AS} = 3.3 V ± 5%, V_{DS} = 3.3 V ± 10%, f_{OSCIN} = 27 MHz, f_{SYSCLK} = 216 MHz, f_{MCLK} = 54 MHz (M = 8), ADC Clock from OSCIN, R_{SET} = 4.02 kΩ, 75 Ω DAC Load)

Parameter	Temp	Test Level	Min	Typ	Max	Unit
OSCIN AND XTAL CHARACTERISTICS						
Frequency Range	Full	II	3		29	MHz
Duty Cycle	Full	II	35	50	65	%
Input Impedance	25°C	III		100||3		MΩ||pF
MCLK Cycle to Cycle Jitter	25°C	III		6		ps rms
Tx DAC CHARACTERISTICS						
Resolution	N/A	N/A		12		Bits
Maximum Sample Rate	Full	II	232			MHz
Full-Scale Output Current	Full	II	4	10	20	mA
Gain Error (Using Internal Reference)	Full	II	–2.0	–1.0	+2.0	%FS
Offset Error	25°C	III		±1.0		%FS
Reference Voltage (REFIO Level)	25°C	III		1.23		V
Differential Nonlinearity (DNL)	25°C	III		±2.5		LSB
Integral Nonlinearity (INL)	25°C	III		±8		LSB
Output Capacitance	25°C	III		5		pF
Phase Noise @ 1 kHz Offset, 42 MHz						
Crystal and OSCIN Multiplier Enabled at 16 ×	25°C	III		–110		dBc/Hz
Output Voltage Compliance Range	Full	II	–0.5		+1.5	V
Wideband SFDR						
5 MHz Analog Out, I_{OUT} = 10 mA	Full	I	60.8	66.9		dBc
65 MHz Analog Out, I_{OUT} = 10 mA	Full	I	44.0	46.2		dBc
Narrow-band SFDR (±1 MHz Window):						
5 MHz Analog Out, I_{OUT} = 10 mA	Full	I	65.4	72.3		dBc
Tx MODULATOR CHARACTERISTICS						
I/Q Offset	Full	II	50	55		dB
Pass-Band Amplitude Ripple ($f < f_{IQCLK}/8$)	Full	II			±0.1	dB
Pass-Band Amplitude Ripple ($f < f_{IQCLK}/4$)	Full	II			±0.5	dB
Stop-Band Response ($f > f_{IQCLK} \times 3/4$)	Full	II			–63	dB
Tx GAIN CONTROL						
Gain Step Size	25°C	III		0.5		dB
Gain Step Error	25°C	III		<0.05		dB
Settling Time to 1% (Full-Scale Step)	25°C	III		1.8		µs
IQ ADC CHARACTERISTICS						
Resolution*	N/A	N/A		6		Bits
Maximum Conversion Rate	Full	III	14.5			MHz
Pipeline Delay	N/A	N/A		3.5		ADC Cycles
Offset Matching between I and Q ADCs				±4.0		LSBs
Gain Matching between I and Q ADCs				±2.0		LSBs
Analog Input						
Input Voltage Range*	Full	III		1		Vppd
Input Capacitance	25°C	III		2.0		pF
Differential Input Resistance	25°C	III		4		kΩ
AC Performance (A_{IN} = 0.5 dBFS, f_{IN} = 5 MHz)						
Effective Number of Bits (ENOB)	Full	I	5.25	5.8		Bits
Signal-to-Noise Ratio (SNR)	Full	I		36.5		dB
Total Harmonic Distortion (THD)	Full	I		–50		dB
Spurious-Free Dynamic Range (SFDR)	Full	I		51		dB

*IQ ADC in Default Mode. ADC Clock Select Register 8, Bit 3 set to "0."

Parameter	Temp	Test Level	Min	Typ	Max	Unit
10-BIT ADC CHARACTERISTICS						
Resolution	N/A	N/A		10		Bits
Maximum Conversion Rate	Full	II	29			MHz
Pipeline Delay	N/A	N/A		4.5		ADC Cycles
Analog Input						
Input Voltage Range	Full	III		2.0		Vppd
Input Capacitance	25°C	III		2		pF
Differential Input Resistance	25°C	II		4		kΩ
Reference Voltage Error						
(REFT10–REFB10) –1 V	Full	I		±4	±200	mV
AC Performance (A_{IN} = –0.5 dBFS, f_{IN} = 5 MHz)						
ADC Sample Clock Source = OSCIN						
Signal-to-Noise and Distortion (SINAD)	Full	I	58.3	59.9		dB
Effective Number of Bits (ENOB)	Full	I	9.4	9.65		Bits
Signal-to-Noise Ratio (SNR)	Full	I	58.6	60		dB
Total Harmonic Distortion (THD)	Full	I		–73	–62	dB
Spurious-Free Dynamic Range (SFDR)	Full	I	65.7	76		dB
AC Performance (A_{IN} = –0.5 dBFS, f_{IN} = 50 MHz)						
ADC Sample Clock Source = OSCIN						
Signal-to-Noise and Distortion (SINAD)	Full	II	57.7	59.0		dB
Effective Number of Bits (ENOB)	Full	II	9.29	9.51		Bits
Signal-to-Noise Ratio (SNR)	Full	II	57.8	59.1		dB
Total Harmonic Distortion (THD)	Full	II	+57	–75		dB
Spurious-Free Dynamic Range (SFDR)	Full	II	64	78		dB
12-BIT ADC CHARACTERISTICS						
Resolution	N/A	N/A		12		Bits
Maximum Conversion Rate	Full	II	29			MHz
Pipeline Delay	N/A	N/A		5.5		ADC Cycles
Analog Input						
Input Voltage Range	Full	III		2		Vppd
Input Capacitance	25°C	III		2		pF
Differential Input Resistance	25°C	III		4		kΩ
Reference Voltage Error						
(REFT12–REFB12) –1 V	Full	I		±16	±200	mV
AC Performance (A_{IN} = –0.5 dBFS, f_{IN} = 5 MHz)						
ADC Sample Clock Source = OSCIN						
Signal-to-Noise and Distortion (SINAD)	Full	I	60.0	65.2		dB
Effective Number of Bits (ENOB)	Full	I	9.67	10.53		Bits
Signal-to-Noise Ratio (SNR)	Full	I	60.3	65.6		dB
Total Harmonic Distortion (THD)	Full	I		–76.6	–58.7	dB
Spurious-Free Dynamic Range (SFDR)	Full	I	64.7	79		dB
AC Performance (A_{IN} = –0.5 dBFS, f_{IN} = 50 MHz)						
ADC Sample Clock Source = OSCIN						
Signal-to-Noise and Distortion (SINAD)	Full	II	59.5	62.7		dB
Effective Number of Bits (ENOB)	Full	II	9.59	10.1		Bits
Signal-to-Noise Ratio (SNR)	Full	II	59.7	63.0		dB
Total Harmonic Distortion (THD)	Full	II		–75.5	–60.5	dB
Spurious-Free Dynamic Range (SFDR)	Full	II	63.8	79		dB

Parameter	Temp	Test Level	Min	Typ	Max	Unit
CHANNEL-TO-CHANNEL ISOLATION						
Tx DAC-to-ADC Isolation (A_{OUT} = 5 MHz)						
Isolation between Tx and IQ ADCs	25°C	III		>60		dB
Isolation between Tx and 10-Bit ADC	25°C	III		>80		dB
Isolation between Tx and 12-Bit ADC	25°C	III		>80		dB
ADC-to-ADC (A_{IN} = –0.5 dBFS, f = 5 MHz)						
Isolation between IF10 and IF12 ADCs	25°C	III		>85		dB
Isolation between Q and I Inputs	25°C	III		>50		dB
TIMING CHARACTERISTICS (10 pF Load)						
Minimum RESET Pulsewidth Low (t_{RL})	N/A	N/A	5			t_{MCLK} Cycles
Digital Output Rise/Fall Time	Full	II	2.8		4	ns
Tx/Rx Interface						
MCLK Frequency (f_{MCLK})	Full	II			66	MHz
TxSYNC/TxIQ Setup Time (t_{SU})	Full	II	3			ns
TxSYNC/TxIQ Hold Time (t_{HD})	Full	II	3			ns
MCLK Rising Edge to						
RxSYNC/RxIQ/IF Valid Delay (t_{MD})	Full	II	0		1.0	ns
OSCOUT Rising or Falling Edge to						
RxSYNC/RxIQ/IF Valid Delay (t_{OD})	Full	II	$T_{OSC}/4 - 2.0$		$T_{OSC}/4 + 3.0$	ns
OSCOUT Edge to MCLK Falling Edge (t_{EE})	Full	II	–1.0		+1.0	ns
Serial Control Bus						
Maximum SCLK Frequency (f_{SCLK})	Full	II			15	MHz
Minimum Clock Pulsewidth High (t_{PWH})	Full	II	30			ns
Minimum Clock Pulsewidth Low (t_{PWL})	Full	II	30			ns
Maximum Clock Rise/Fall Time	Full	II			1	ms
Minimum Data/Chip-Select Setup Time (t_{DS})	Full	II	25			ns
Minimum Data Hold Time (t_{DH})	Full	II	0			ns
Maximum Data Valid Time (t_{DV})	Full	II			30	ns
CMOS LOGIC INPUTS						
Logic “1” Voltage	25°C	II	$V_{DRVDD} - 0.7$			V
Logic “0” Voltage	25°C	II			0.4	V
Logic “1” Current	25°C	II			12	µA
Logic “0” Current	25°C	II			12	µA
Input Capacitance	25°C	II		3		pF
CMOS LOGIC OUTPUTS (1 mA Load)						
Logic “1” Voltage	25°C	II	$V_{DRVDD} - 0.6$			V
Logic “0” Voltage	25°C	II			0.4	V
POWER SUPPLY						
Supply Current, I_S (Full Operation)	25°C	II		163	178	mA
Analog Supply Current, I_{AS}	25°C	III		95		mA
Digital Supply Current, I_{DS}	25°C	III		68		mA
Supply Current, I_S						
Standby ($\overline{PWRDN}$ Pin Active)	25°C	II		119	123	mA
Full Power-Down (Register 2 = 0xF9)	25°C	III		16		mA
Power-Down Tx Path (Register 2 = 0x60)	25°C	III		113		mA
Power-Down Rx Paths (Register 2 = 0x19)	25°C	III		110		mA

ABSOLUTE MAXIMUM RATINGS*

Power Supply (V_{AVDD},V_{DVDD},V_{DRVDD}) . . . . . 3.9 V
Digital Output Current . . . . . 5 mA
Digital Inputs . . . . . –0.3 V to V_{DRVDD} + 0.3 V
Analog Inputs . . . . . –0.3 V to V_{AVDD} + 0.3 V
Operating Temperature . . . . . –40°C to +85°C
Maximum Junction Temperature . . . . . 150°C
Storage Temperature . . . . . –65°C to +150°C
Lead Temperature (Soldering 10 sec) . . . . . 300°C

*Absolute Maximum Ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

EXPLANATION OF TEST LEVELS

I. Devices are 100% production tested at +25°C and guaranteed by design and characterization testing for commercial operating temperature range (–40°C to +85°C).

II. Parameter is guaranteed by design and/or characterization testing.

III. Parameter is a typical value only.

N/A Test level definition is not applicable.

ORDERING GUIDE

Model	Temperature Range	Package Description
AD9879BS	–40°C to +85°C	100-Lead MQFP

THERMAL CHARACTERISTICS

Thermal Resistance

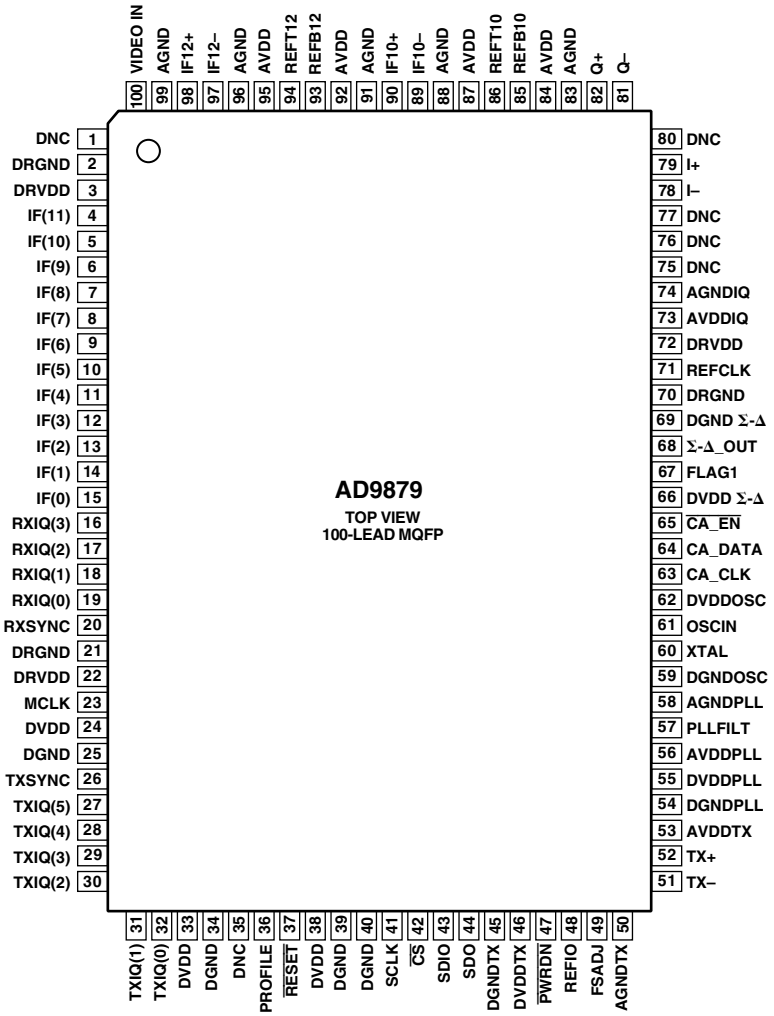
100-Lead MQFP

θ_{JA} = 40.5°C/W

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9879 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION ASSIGNMENTS

Pin No.	Mnemonic	Pin Function
1, 35, 75–77, 80	DNC	Do Not Connect. Pins are not bonded to die.
2, 21, 70	DRGND	Pin Driver Digital Ground
3, 22, 72	DRVDD	Pin Driver Digital 3.3 V Supply
4–15	IF[11:0]	12-Bit ADC Digital Output
16–19	RXIQ[3:0]	Muxed I and Q ADCs Output
20	RXSYNC	Sync Output, IF, I and Q ADCs
23	MCLK	Master Clock Output
24, 33, 38	DVDD	Digital 3.3 V Supply
25, 34, 39, 40	DGND	Digital Ground
26	TXSYNC	Sync Input for Transmit Port
27–32	TXIQ[5:0]	Digital Input for Transmit Port
36	PROFILE	Profile Selection Inputs
37	$\overline{\text{RESET}}$	Chip Reset Input (Active Low)
41	SCLK	SPORT Clock
42	$\overline{\text{CS}}$	SPORT Chip Select
43	SDIO	SPORT Data I/O
44	SDO	SPORT Data Output
45	DGNDTX	Tx Path Digital Ground
46	DVDDTX	Tx Path Digital 3.3 V Supply
47	$\overline{\text{PWRDN}}$	Power-Down Transmit Path
48	REFIO	TxDAC Decoupling (to AGND)
49	FSADJ	DAC Output Adjust (External Res.)
50	AGNDTX	Tx Path Analog Ground
51, 52	TX–, TX+	Tx Path Complementary Outputs
53	AVDDTX	Tx Path Analog 3.3 V Supply
54	DGNDPLL	PLL Digital Ground
55	DVDDPLL	PLL Digital 3.3 V Supply
56	AVDDPLL	PLL Analog 3.3 V Supply
57	PLLFILT	PLL Loop Filter Connection
58	AGNDPLL	PLL Analog Ground
59	DGNDOSC	Oscillator Digital Ground
60	XTAL	Crystal Oscillator Inv. Output
61	OSCIN	Oscillator Clock Input
62	DVDDOSC	Oscillator Digital 3.3 V Supply
63	CA_CLK	Serial Clock to Cable Driver
64	CA_DATA	Serial Data to Cable Driver
65	$\overline{\text{CA\_EN}}$	Serial Enable to Cable Drive
66	DVDD Σ-Δ	Sigma Delta Digital 3.3 V Supply
67	FLAG1	Digital Output Flag 1
68	Σ-Δ _OUT	Sigma-Delta DAC Output
69	DGND Σ-Δ	Sigma-Delta Digital Ground
71	REFCLK	Oscillator Clock Output
73	AVDDIQ	7-Bit ADCs Analog 3.3 V Supply
74	AGNDIQ	7-Bit ADCs Analog Ground
78, 79	I–, I+	Differential Input to I ADC
81, 82	Q–, Q+	Differential Input to Q ADC
83, 88, 91, 96, 99	AGND	12-Bit ADC Analog Ground
84, 87, 92, 95	AVDD	12-Bit ADC Analog 3.3 V Supply
85	REFB10	10-Bit ADC Decoupling Node
86	REFT10	10-Bit ADC Decoupling Node
89, 90	IF10–, IF10+	Differential Input to 10-Bit ADC
93	REFB12	12-Bit ADC Decoupling Node
94	REFT12	12-Bit ADC Decoupling Node
97, 98	IF12–, IF12+	Differential Input to IF ADC
100	VIDEO IN	Video Clamp Input, 12-Bit ADC

DEFINITIONS OF SPECIFICATIONS

Differential Nonlinearity Error (DNL, NO MISSING CODES)
An ideal converter exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to 10-bit resolution indicates that all 1024 codes, respectively, must be present over all operating ranges.

Integral Nonlinearity Error (INL)
Linearity error refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs 1/2 LSB before the first code transition. Positive full scale is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

Phase Noise
Single-sideband phase noise power is specified relative to the carrier (dBc/Hz) at a given frequency offset (1 kHz) from the carrier. Phase noise can be measured directly in single-tone transmit mode with a spectrum analyzer that supports noise marker measurements. It detects the relative power between the carrier and the offset (1 kHz) sideband noise and takes the resolution bandwidth (rbw) into account by subtracting 10log(rbw). It also adds a correction factor that compensates for the implementation of the resolution bandwidth, log display, and detector characteristic.

Output Compliance Range
The range of allowable voltage at the output of a current output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown, resulting in nonlinear performance.

Spurious-Free Dynamic Range (SFDR)
The difference, in dB, between the rms amplitude of the DAC output signal (or the ADC input signal) and the peak spurious signal over the specified bandwidth (Nyquist bandwidth unless otherwise noted).

Pipeline Delay (Latency)
The number of clock cycles between conversion initiation and the associated output data being made available.

Offset Error
First transition should occur for an analog value 1/2 LSB above –FS. Offset error is defined as the deviation of the actual transition from that point.

Gain Error
The first code transition should occur at an analog value 1/2 LSB above full scale. The last transition should occur at an analog value 1 1/2 LSB below the nominal full scale. Gain error is the deviation of the actual difference between the first and last code transitions and the ideal difference between the first and last code transitions.

Aperture Delay
The aperture delay is a measure of the sample-and-hold amplifier (SHA) performance and specifies the time delay between the rising edge of the sampling clock input to when the input signal is held for conversion.

Aperture Uncertainty (Jitter)
Aperture jitter is the variation in aperture delay for successive samples and is manifested as noise on the input to the ADC.

Input Reference Noise
The rms output noise is measured using histogram techniques. The ADC output codes' standard deviation is calculated in LSB and converted to an equivalent voltage. This results in a noise figure that can directly be referred to the input of the MxFE.

Signal-To-Noise and Distortion (S/N+D, SINAD) Ratio
SINAD is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Effective Number of Bits (ENOB)
For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula:

$$N = (SINAD - 1.76)dB/6.02$$

it is possible to get a performance measurement expressed as N, the effective number of bits. Thus, effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

Signal-To-Noise Ratio (SNR)
SNR is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

Power Supply Rejection
Power supply rejection specifies the converter's maximum full-scale change when the supplies are varied from nominal to minimum and maximum specified voltages.

Channel-To-Channel Isolation (Crosstalk)
In an ideal multichannel system, the signal in one channel will not influence the signal level of another channel. The channel-to-channel isolation specification is a measure of the change that occurs to a grounded channel as a full-scale signal is applied to another channel.

Table I. Register Map

Address (hex)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default (hex)	Type
00h	SDIO Bidirectional	SPI Bytes LSB First	Reset	OSCIN Multiplier M[4:0]					0x08	Read/Write
01h	PLL Lock Detect		MCLK/REFCLK Ratio R[5:0]						0x00	Read/Write
02h	Power-Down PLL	Power-Down DAC Tx	Power-Down Digital Tx	Power-Down IF12 ADC	Power-Down Reference IF12 ADC	Power-Down IF10 ADC	Power-Down Reference IQ and IF10 ADC	Power-Down IQ ADC	0x00	Read/Write
03h	Sigma-Delta Output Control Word [3:0]						Flag 1	Flag 0 Enable	0x00	Read/Write
04h	Flag 0	Sigma-Delta Output Control Word [11:4]							0x00	Read/Write
05h	0	0	0	0	0	0	0	0	0x00	Read/Write
06h	0	0	0	0	0	0	0	0	0x00	Read-Only
07h	Video Input Enable	Clamp Level for Video Input [6:0]							0x00	Read/Write
08h	ADCs Clocked Direct from OSCIN	0	Rx Port Fast Edge Rate	Power-Down RxSYNC and IQ ADC Clocks	Enable 7-Bits IQ ADC	0	Send 12-Bit ADC Data Only	Send 10-Bit ADC Data Only	0x80	Read/Write
09h	0	0	0	0	0	0	0	0	0x00	Read/Write
0Ah	0	0	0	0	0	0	0	0	0x00	Read/Write
0Bh	0	0	0	0	0	0	0	0	0x00	Read/Write
0Ch	0	0	0	0	Version [3:0]				0x05	Read/Write
0Dh	0	0	0	0	Tx Frequency Tuning Word Profile 1 LSBs [1:0]		Tx Frequency Tuning Word Profile 0 LSBs [1:0]		0x00	Read/Write
0Eh	0	0	0	0	DAC Fine Gain Control [3:0]				0x00	Read/Write
0Fh	0	0	Tx Path Select Profile 1	0	Tx Path AD8322/ AD8327 Gain Control Mode	Tx Path Bypass Sinc^{-1} Filter	Tx Path Spectral Inversion	Tx Path Transmit Single Tone	0x00	Read/Write
10h	Tx Path Frequency Tuning Word Profile 0 [9:2]								0x00	Read/Write
11h	Tx Path Frequency Tuning Word Profile 0 [17:10]								0x00	Read/Write
12h	Tx Path Frequency Tuning Word Profile 0 [25:18]								0x00	Read/Write
13h	Cable Driver Amplifier Coarse Gain Control Profile 0 [7:4]					Fine Gain Control Profile 0 [3:0]			0x00	Read/Write
14h	Tx Path Frequency Tuning Word Profile 1 [9:2]								0x00	Read/Write
15h	Tx Path Frequency Tuning Word Profile 1 [17:10]								0x00	Read/Write
16h	Tx Path Frequency Tuning Word Profile 1 [25:18]								0x00	Read/Write
17h	Cable Driver Amplifier Coarse Gain Control Profile 1 [7:4]					Fine Gain Control Profile 1 [3:0]			0x00	Read/Write

Register bits denoted with "0" MUST be programmed with a "0" every time that register is written.

REGISTER BIT DEFINITIONS

Register 00 — Initialization

Bits 0 to 4: OSCIN Multiplier

This register field is used to program the on-chip multiplier (PLL) that generates the chip's high frequency system clock f_{SYSCLK}. The value of M will depend on the ADC clocking mode selected as shown in the table below.

Table II.

ADC Clock Select	M
1, f_{OSCIN}	8
0, f_{MCLK} (PLL Derived)	16

When using the AD9879 in systems where the Tx path and Rx path do not operate simultaneously, the value of M can be programmed from 1 to 31. The maximum f_{SYSCLK} rate of 236 MHz must be observed, whatever value is chosen for M. When M is set to 1, the internal PLL is disabled and all internal clocks are derived directly from OSCIN.

Bit 5: Reset

Writing a 1 to this bit resets the registers to their default values and restarts the chip. The Reset bit always reads back 0. The bits in Register 0 are not affected by this software reset. However, a low level at the $\overline{\text{RESET}}$ pin would force all registers, including all bits in Register 0, to their default state.

Bit 6: SPI Bytes LSB First

Active high indicates SPI serial port access of instruction byte and data registers is least significant bit (LSB) first. Default low indicates most significant bit (MSB) first format.

Bit 7: SDIO Bidirectional

Active high configures the serial port as a three signal port with the SDIO pin used as a bidirectional input/output pin. Default low indicates the serial port uses four signals with SDIO configured as an input and SDO configured as an output.

Register 01 — Clock Configuration

Bits 0 to 5: MCLK/REFCLK Ratio

This bit field defines, R, the ratio between the auxiliary clock output, REFCLK and MCLK. R can be any integer number between 2 and 63. At default zero (R = 0), REFCLK provides a buffered version of the OSCIN clock signal.

Bit 7: PLL Lock Detect

When this bit is set low, the REFCLK pin functions in its default mode, and provides an output clock with frequency f_{MCLK}/R as described above.

If this bit is set to 1, the REFCLK pin is configured to indicate whether the PLL is locked to f_{OSCIN}. In this mode, the REFCLK pin should be low-pass filtered with an RC filter of 1.0 kΩ and 0.1 µF. A high output on REFCLK indicates that the PLL has achieved lock with f_{OSCIN}.

Register 02 — POWER-DOWN

Sections of the chip that are not used can be powered down when the corresponding bits are set high. This register has a default value of 0x00; all sections active.

Bit 0: Power-Down IQ ADC

Active high powers down the IQ ADC.

Bit 1: Power-Down IQ and IF10 ADC Reference

Active high powers down the IQ and IF10 ADC reference.

Bit 2: Power-Down IF10 ADC

Active high powers down the IF10 ADC.

Bit 3: Power-Down IF12 ADC Reference

Active high powers down the 12-bit ADC reference.

Bit 4: Power-Down IF12 ADC

Active high powers down the IF12 ADC.

Bit 5: Power-Down Digital TX

Active high powers down the digital transmit section of the chip, similar to the function of the PWRDN Pin.

Bit 6: Power-Down DAC TX

Active high powers down the DAC.

Bit 7: Power-Down PLL

Active high powers down the OSCIN multiplier.

Registers 03 and 04 — Sigma-Delta and Flag Control

The sigma-delta control word is 12 bits wide and split in MSB bits [11:4] and LSB bits [3:0]. Changes to the sigma-delta control words take effect immediately for every MSB or LSB register write. Sigma-delta output control words have a default value of "0." The control words are in straight binary format with 0x000 corresponding to the bottom of the scale and 0xFFF corresponding to the top of the scale. See Figure 6 for details.

If the Flag 0 Enable (Register 3, Bit 0) is set high, the Σ-Δ_OUT pin will maintain a fixed logic level determined directly by the MSB of the sigma-delta control word.

The FLAG1 pin assumes the logic level programmed into the FLAG1 bit (Register 3, Bit 1).

Register 07 —VIDEO INPUT CONFIGURATION

Bits 0-6: Clamp Level Control Value

The 7-bit clamp level control value is used to set an offset to the automatic clamp level control loop. The actual ADC output will have a clamp level offset equal to 16 times the clamp level control value as shown:

$$Clamp\ Level\ Offset = Clamp\ Level\ Control\ Value\ (\times)\ 16$$

The default value for the clamp level control value is 0x20. This results in an ADC output clamp level offset of 512 LSBs. The valid programming range for the clamp level control value is from 0x16 to 0x127.

Register 08 — ADC CLOCK CONFIGURATION

Bit 0: Send 10-Bit ADC Data Only

When this bit is set high, the device enters a Nonmultiplexed mode and only the data from the 10-bit ADC will be sent to the IF [11:0] digital output port.

Bit 1: Send 12-Bit ADC Data Only

When this bit is set high, the device enters a Nonmultiplexed mode and only data from the 12-bit ADC will be sent to the IF [11:0] digital output port.

Bit 3: Enable 7-Bits, IQ ADC

When this bit is active the IQ ADC is put into 7-bit mode. In this mode, the full-scale input range is 2 Vppd. When this bit is set inactive, the IQ ADC is put into 6-bit mode and the full-scale input voltage range is 1 Vppd.

Bit 4: Power-Down RXSYNC and IQ ADC Clocks

Setting this bit to 1 powers down the IQ ADC's sampling clock and stops the RXSYNC output pin. It can be used for additional power saving on top of the power-down selections in Register 2.

Bit 5: Rx Port Fast Edge Rate
Setting this bit to 1 increases the output drive strength of all digital output pins, except MCLK, REFCLK, Σ-Δ_OUT, and FLAG1. These pins always have high output drive capability.

Bit 7: ADC Clocked Direct from OSCIN
When set high, the input clock at OSCIN is used directly as the ADC sampling clock. When set low, the internally generated master clock, MCLK, is divided by two and used as the ADC sampling clock. Best ADC performance is achieved when the ADCs are sampled directly from f_{OSCIN} using an external crystal or low jitter crystal oscillator.

Register C—DIE REVISION
Bits 0 to 3: Version
The die version of the chip can be read from this register.

Register D—Tx Frequency Tuning Words LSBs
This register accommodates two least significant bits for both of the frequency tuning words. See description of Carrier Frequency Tuning.

Register E—DAC Gain Control
Bits 0 to 3: DAC Fine Gain Control
This bit field sets the DAC gain if the Tx Path AD8321/AD8323 Gain Control Select bit (Register F, Bit 3) is set to 0. The DAC gain can be set from 0.0 dB to 7.5 dB in increments of 0.5 dB. Table III details the programming.

Table III.

Bits [3:0]	DAC Gain
0000	0.0 dB (Default)
0001	0.5 dB
0010	1.0 dB
0011	1.5 dB
....	....
1110	7.0 dB
1111	7.5 dB

Register F — Tx PATH CONFIGURATION
Bit 0: Tx Path Transmit Single Tone
Active high configures the AD9879 for single-tone applications (e.g., FSK). The AD9879 will supply a single frequency output as determined by the frequency tuning word selected by the active profile. In this mode, the TXIQ input data pins are ignored but should be tied to a valid logic voltage level. Default value is 0 (inactive).

Bit 1: Tx Path Spectral Inversion
When set to 1, inverted modulation is performed:

$$MODULAR\_OUT = \left[I\ cos\left(\omega t\right) + Q\ sin\left(\omega t\right)\right]$$

Default is logic zero, noninverted modulation:

$$MODULAR\_OUT = \left[I\ cos\left(\omega t\right) + Q\ sin\left(\omega t\right)\right]$$

Bit 2: Tx Path Bypass Sinc^{-1} Filter
Setting this bit high bypasses the digital inverse sinc filter of the Tx path.

Bit 3: Tx Path AD8322/AD8327 Gain Control Mode
This bit changes the manner in which transmit gain control is performed. Typically either AD8321/AD8323 (default 0) or AD8222/AD8327 (default 1) variable gain cable drivers are programmed over the chip's 3-wire CA interface. The Tx gain control select changes the interpretation of the bits in Registers 13 and 17. See Cable Driver Gain Control.

Bit 5: Tx Path Select Profile 1
The AD9879 quadrature digital upconverter is capable of storing two preconfigured modulation modes called profiles. Each profile defines a transmit frequency tuning word and cable driver amplifier gain (/DAC gain) setting. The Profile Select bit or PROFILE pin programs the current register profile to be used. The Profile Select bit should always be "0" if the PROFILE pin is to be used to switch between profiles. Using the Profile Select bit as a means of switching between different profiles requires the PROFILE pin to be tied low.

Registers 10–17: Carrier Frequency Tuning
Tx Path Frequency Tuning Words
The frequency tuning word (*FTW*) determines the DDS-generated carrier frequency (f_C) and is formed via a concatenation of register addresses.

The 26-bit *FTW* is spread over four register addresses. Bit 25 is the MSB and Bit 0 is the LSB.

The carrier frequency equation is given as:

$$f_C = \left[FTW \times f_{SYSCLK}\right] / 2^{26}$$

where $f_{SYSCLK} = M \times f_{OSCIN}$ *and* $FTW < 0 \times 2000000$

Changes to *FTW* bytes take effect immediately.

Cable Driver Gain Control
The AD9879 has a 3-pin interface to the AD832x family of programmable gain cable driver amplifiers. This allows direct control of the cable driver's gain through the AD9879.

In its Default mode, the complete 8-bit register value is transmitted over the 3-wire cable amplifier (CA) interface.

If Bit 3 of Register F is set high, Bits [7:4] determine the 8-bit word sent over the CA interface according to Table IV.

Table IV.

Bits [7:4]	CA Interface Transmit Word
0000	0000 0000 (Default)
0001	0000 0001
...	...
0111	0100 0000
1000	1000 0000

In this mode, the lower bits determine the fine gain setting of the DAC output.

Table V.

Bits [3:0]	DAC Fine Gain
0000	0.0 dB (Default)
0001	0.5 dB
...	...
1110	7.0 dB
1111	7.5 dB

New data is automatically sent over the 3-wire CA interface (and DAC gain adjust) whenever the value of the active gain control register changes or a new profile is selected. The default value is 0x00 (lowest gain).

The formula for the combined output level calculation of the AD9879 fine gain and AD8327 or AD8322 coarse gain is:

$$V_{8327} = V_{9877(0)} + (fine)/2 + 6(coarse) - 19$$

$$V_{8322} = V_{9877(0)} + (fine)/2 + 6(coarse) - 14$$

with:

fine = decimal value of Bits [3:0]
coarse = decimal value of Bits [7:8]

$V_{9877(0)}$: Level at AD9879 output in dBmV for fine = 0.
V_{8327}: Level at output of AD8327 in dBmV.
V_{8322}: Level at output of AD8322 in dBmV.

DEVICE OVERVIEW

To gain a general understanding of the AD9879, it is helpful to refer to Figure 1, which displays a block diagram of the device architecture. The device consists of a transmit path, receive path, and auxiliary functions, such as a DPLL, a sigma-delta DAC, a serial control port, and a cable amplifier interface.

Transmit Path

The transmit path contains an interpolation filter, a complete quadrature digital upconverter, an inverse sinc filter, and a 12-bit current output DAC. The maximum output current of the DAC is set by an external resistor. The Tx output PGA provides additional transmit signal level control.

The transmit path interpolation filter provides an upsampling factor of 16 with an output signal bandwidth as high as 5.8 MHz. Carrier frequencies up to 65 MHz with 26 bits of frequency tuning resolution can be generated by the direct digital synthesizer (DDS). The transmit DAC resolution is 12 bits and can run at sampling rates as high as 232 MSPS.

Analog output scaling from 0 dB to 7.5 dB in 0.5 dB steps is available to preserve SNR when reduced output levels are required.

Data Assembler

The AD9879 data path operates on two 12-bit words, the I and Q components, that form a complex symbol. The data assembler builds the 24-bit complex symbols from four consecutive 6-bit nibbles read over the TxIQ[5:0] bus. The nibbles are strobed synchronous to the master clock, MCLK, into the data assembler. A high level on TxSYNC signals the start of a transmit symbol. The first two nibbles of the symbol form the I component, the second two nibbles form the Q component. Symbol components are assumed to be in twos complement format. The timing of the interface is fully described in the Transmit Timing section of this data sheet.

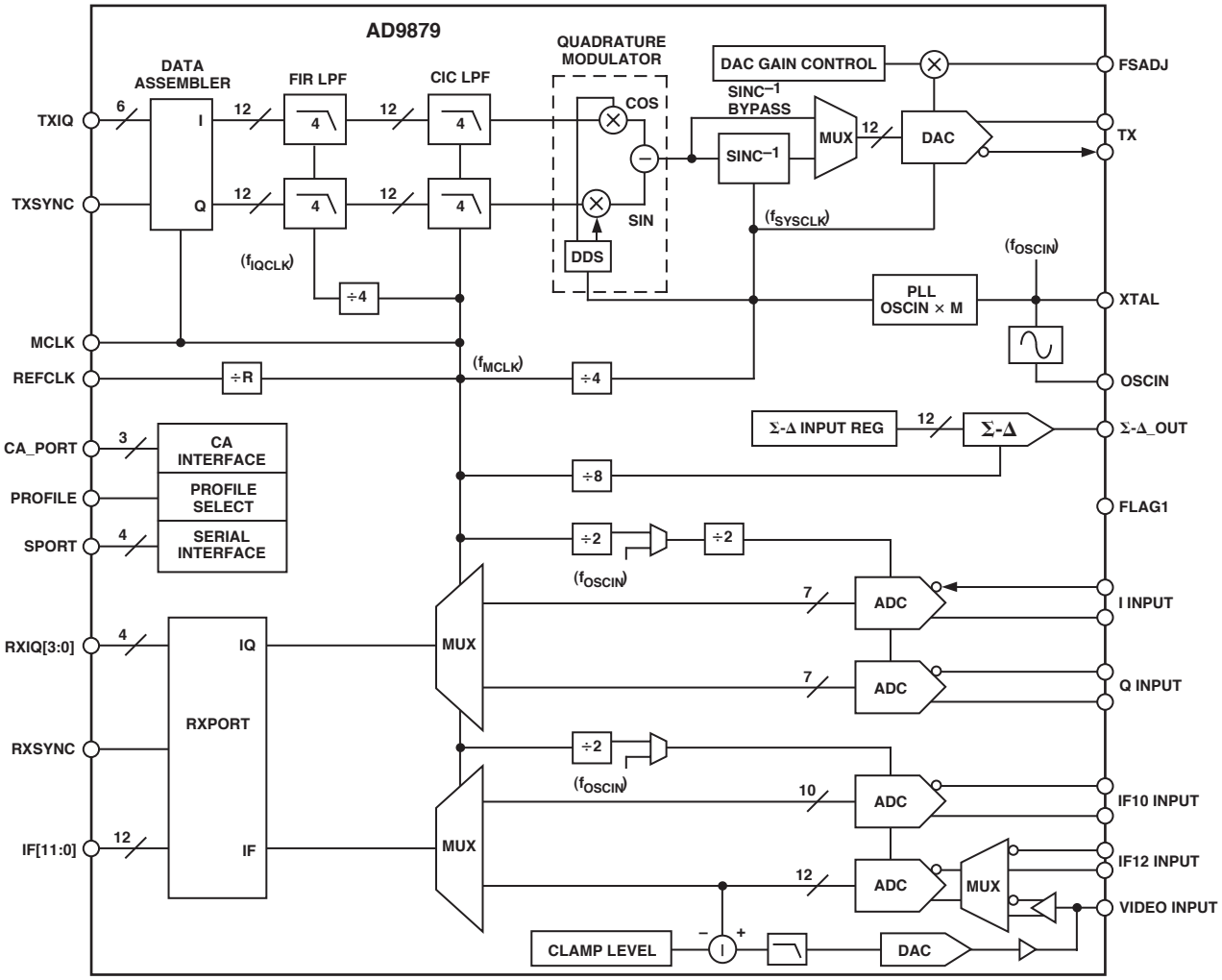


Figure 1. Block Diagram

INTERPOLATION FILTER

Once through the Data Assembler, the IQ data streams are fed through a 4× FIR low-pass filter and a 4× Cascaded Integrator-Comb (CIC) low-pass filter. The combination of these two filters results in the sample rate increasing by a factor of 16. In addition to the sample rate increase, the half-band filters provide the low-pass filtering characteristic necessary to suppress the spectral images between the original sampling frequency and the new (16× higher) sampling frequency.

DIGITAL UPCONVERTER

The digital quadrature modulator stage following the CIC filters is used to frequency shift (upconvert) the baseband spectrum of the incoming data stream up to the desired carrier frequency. The carrier frequency is controlled numerically by a Direct Digital Synthesizer (DDS). The DDS uses the internal system clock (f_{SYSCLK}) to generate the desired carrier frequency with a high degree of precision. The carrier is applied to the I and Q multipliers in quadrature fashion (90° phase offset) and summed to yield a data stream that is the modulated carrier. The modulated carrier becomes the 12-bit sample sent to the DAC.

The receive path contains a 12-bit ADC, a 10-bit ADC, and a dual 7-bit ADC. All internally required clocks and an output system clock are generated by the PLL from a single crystal or clock input.

The 12-bit and 10-bit IF ADCs can convert direct IF inputs up to 70 MHz and run at sample rates up to 33 MSPS. A video input with an adjustable signal clamping level along with the 10-bit ADC allow the AD9879 to process an NTSC and a QAM channel simultaneously.

The programmable sigma-delta DAC can be used to control external components, such as variable gain amplifiers (VGAs) or voltage controlled tuners. The CAPORT provides an interface to the AD8321/AD8323 or AD8322/AD8327 programmable gain amplifier (PGA) cable drivers enabling host processor control via the MxFE SPORT.

OSCIN Clock Multiplier

The AD9879 can accept either an input clock into the OSCIN Pin or a fundamental mode XTAL across the OSCIN Pin and XTAL Pins as the devices main clock source. The internal PLL then generates the f_{SYSCLK} signal from which all other internal signals are derived.

The DAC uses f_{SYSCLK} as its sampling clock. For DDS applications, the carrier is typically limited to about 30% of f_{SYSCLK}. For a 65 MHz carrier, the system clock required is above 216 MHz.

The OSCIN multiplier function maintains clock integrity as evidenced by the AD9879's systems excellent phase noise characteristics and low clock-related spur in the output spectrum. External loop filter components consisting of a series resistor (1.3 kΩ) and capacitor (0.01 μF) provide the compensation zero for the OSCIN multiplier PLL loop. The overall loop performance has been optimized for these component values.

DPLL-A CLOCK DISTRIBUTION

Figure 1 shows the clock signals used in the transmit path. The DAC sampling clock, f_{DAC}, is generated by DPLL-A. F_{DAC} has a frequency equal to the $L \times f_{OSCIN}$, where f_{OSCIN} is the internal signal generated either by the crystal oscillator when a crystal is connected between the OSCIN and XTAL pins, or by the clock that is fed into the OSCIN pin, and L is the multiplier programmed through the serial port. L can have the values of 1, 2, 3, or 8.

The transmit path expects a new half word of data at the rate of f_{CLK-A}. When the Tx multiplexer is enabled, the frequency of Tx Port is:

$$f_{CLK-A} = 2 \times f_{DAC} / K = 2 \times L \times f_{OSCIN} / K$$

where K is the interpolation factor.

The interpolation factor can be programmed to be 1, 2, or 4. When the Tx multiplexer is disabled, the frequency of the Tx Port is:

$$f_{CLK-A} = f_{DAC} / K = L \times f_{OSCIN} / K$$

Receive Section

The AD9879 includes two high speed, high performance ADCs. The 10-bit and 12-bit direct IF ADC's deliver excellent undersampling performance with input frequencies as high as 70 MHz. The sampling rate can be as high as 33 MSPS.

The ADC sampling frequency can be derived directly from the OSCIN signal or from the on-chip OSCIN multiplier. For highest dynamic performance, it is recommended to choose an OSCIN frequency that can directly be used as the ADC sampling clock. Digital IQ ADC outputs are multiplexed to one 4-bit bus, clocked by a frequency (f_{MCLK}) of four times the sampling rate. The IF ADCs use a multiplexed 12-bit interface with an output word rate of f_{MCLK}.

CLOCK AND OSCILLATOR CIRCUITRY

The AD9879's internal oscillator generates all sampling clocks from a simple, low cost, parallel resonance, fundamental frequency quartz crystal. Figure 2 shows how the quartz crystal is connected between OSCIN (Pin 61) and XTAL (Pin 60) with parallel resonant load capacitors as specified by the crystal manufacturer. The internal oscillator circuitry can also be overdriven by a TTL-level clock applied to OSCIN with XTAL left unconnected.

$$f_{OSCIN} = f_{MCLK} \times M$$

An internal phase-locked loop (PLL) generates the DAC sampling frequency, f_{SYSCLK}, by multiplying OSCIN frequency M times. The MCLK signal (Pin 23), f_{MCLK}, is derived by dividing f_{SYSCLK} by 4.

$$f_{SYSCLK} = f_{OSCIN} \times M$$

$$f_{MCLK} = f_{OSCIN} \times M/4$$

An external PLL loop filter (Pin 57) consisting of a series resistor and ceramic capacitor (Figure 15, R1 = 1.3 kΩ, C12 = 0.01 μF) is required for stability of the PLL. Also, a shield surrounding these components is recommended to minimize external noise coupling into the PLL's voltage controlled oscillator input (guard trace connected to AVDDPLL).

Figure 1 shows that ADCs are either sampled directly by a low jitter clock at OSCIN or by a clock that is derived from the PLL output. Operating modes can be selected in Register 8. Sampling the ADCs directly with the OSCIN clock requires MCLK to be programmed to be twice the OSCIN frequency.

PROGRAMMABLE CLOCK OUTPUT REFCLK

The AD9879 provides an auxiliary output clock on Pin 71, REFCLK. The value of the MCLK divider bit field, *R*, determines its output frequency as shown in the equations:

$$f_{REFCLK} = f_{MCLK}/R, \text{ For } R = 2\text{–}63$$

$$f_{REFCLK} = f_{OSCIN}, \text{ For } R = 0$$

In its default setting (0x00 in Register 1), the REFCLK pin provides a buffered output of f_{OSCIN}.

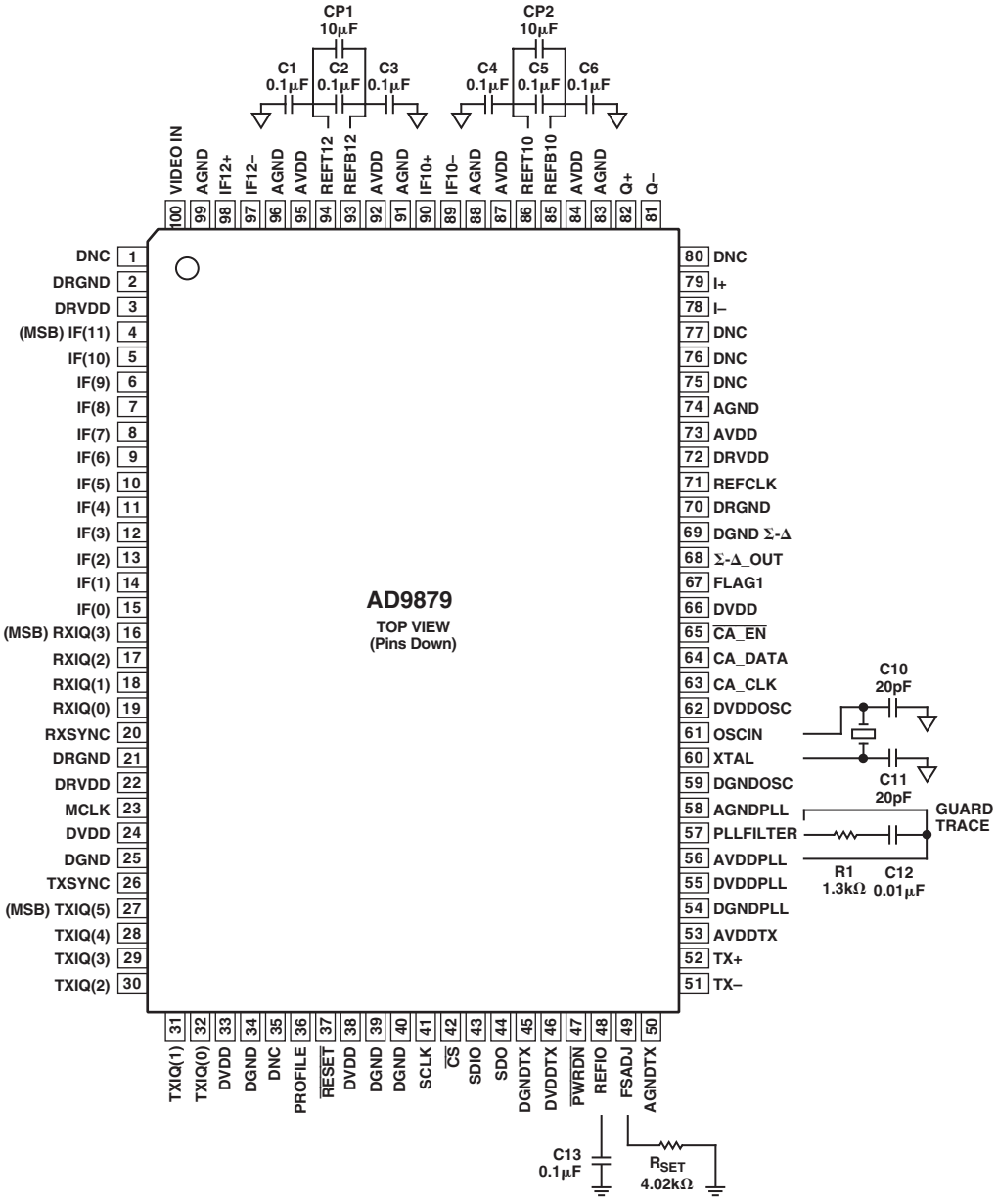


Figure 2. Basic Connection Diagram

RESET AND TRANSMIT POWER-DOWN

Power-Up Sequence

On initial power-up, the $\overline{\text{RESET}}$ pin should be held low until the power supply is stable.

Once $\overline{\text{RESET}}$ is deasserted, the AD9879 can be programmed over the serial port. The on-chip PLL requires a maximum of 1 millisecond after the rising edge of $\overline{\text{RESET}}$ or a change of the multiplier factor (M) to completely settle. It is recommended that the $\overline{\text{PWRDN}}$ pin be held low during the reset and PLL settling time. Changes to ADC Clock Select (Register 08h) or SYS Clock Divider N (Register 01) should be programmed before the rising edge of $\overline{\text{PWRDN}}$.

Once the PLL is frequency locked and after the $\overline{\text{PWRDN}}$ pin is brought high, transmit data can be sent reliably.

If the $\overline{\text{PWRDN}}$ pin cannot be held low throughout the reset and PLL settling time period, then the Power-Down Digital Tx bit or the $\overline{\text{PWRDN}}$ pin should be pulsed after the PLL has settled. This will ensure correct transmit filter initialization.

$\overline{\text{RESET}}$

To initiate hardware reset, the $\overline{\text{RESET}}$ pin should be held low for at least 100 nanoseconds. All internally generated clocks but OSCOUT stop during reset. The rising edge of $\overline{\text{RESET}}$ resets the PLL clock multiplier and reinitializes the programmable registers to their default values. The same sequence as described above in the Power-Up Sequence section should be followed after a reset or change in M.

A software reset (writing a 1 into Bit 5 of Register 00h) is functionally equivalent to the hardware reset but does not force Register 00h to its default value.

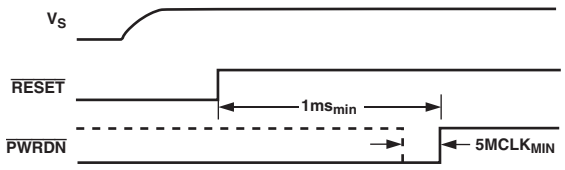


Figure 3. Power-Up Sequence for Tx Data Path

Transmit Power-Down

A low level on the $\overline{\text{PWRDN}}$ pin stops all clocks linked to the digital transmit data path and resets the CIC filter. Deasserting $\overline{\text{PWRDN}}$ reactivates all clocks. The CIC filter is held in a reset state for 80 MCLK cycles after the rising edge of $\overline{\text{PWRDN}}$ to allow for flushing of the half-band filters with new input data.

Transmit data bursts should be padded with at least 20 symbols of null data directly before the $\overline{\text{PWRDN}}$ pin is deasserted. Immediately after $\overline{\text{PWRDN}}$ pin is deasserted, the transmit burst should start with a minimum of 20 null data symbols. This avoids unintended DAC output samples caused by the transmit path latency and filter settling time.

Software Power-Down Digital Tx (Bit 5 in Register 02h) is functionally equivalent to the hardware $\overline{\text{PWRDN}}$ pin and takes effect immediately after the last register bit has been written over the serial port.

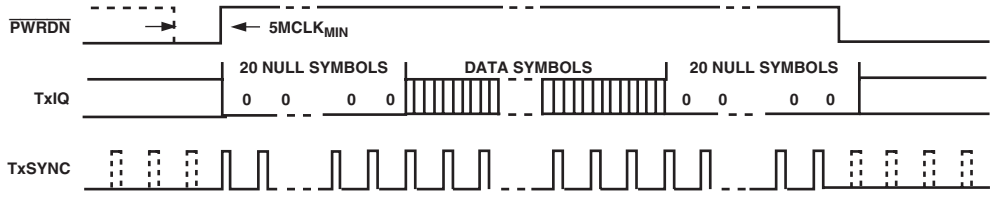


Figure 4. Timing Sequence to Flush Tx Data Path

SIGMA-DELTA OUTPUTS

The AD9879 contains an on-chip sigma-delta output that provides a digital logic bit stream with an average duty cycle that varies between 0% and (4095/4096)%, depending on the programmed code, as shown in Figure 5.

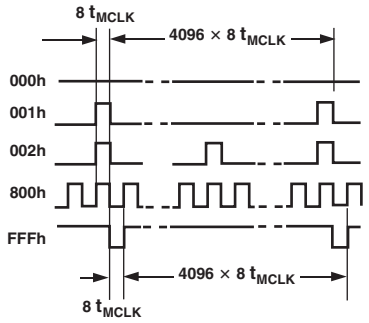


Figure 5. Sigma-Delta Output Signals

This bit stream can be low-pass filtered to generate a programmable dc voltage of:

V_{DC} = (*Sigma-Delta Code*/4096)(V_H) + V_L
where:

$V_H = V_{DRVDD} - 0.6$ V
$V_L = 0.4$ V

In cable modem set-top box applications, the output can be used to control external variable gain amplifiers or RF tuners. A simple single-pole RC low-pass filter provides sufficient filtering (see Figure 6).

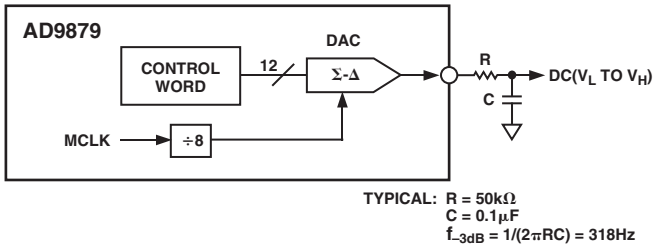


Figure 6. Sigma-Delta RC Filter

In more demanding applications where additional gain, level shift, or drive capability is required, a first or second order active filter might be considered for each sigma-delta output (see Figure 7).

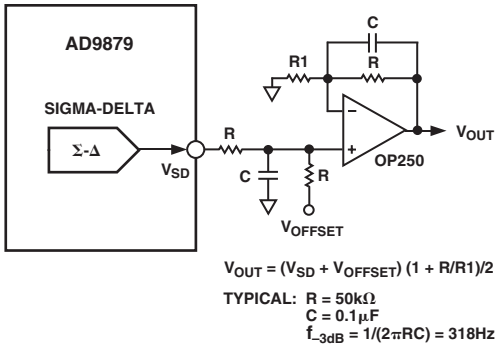


Figure 7. Sigma-Delta Active Filter with Gain and Offset

SERIAL INTERFACE FOR REGISTER CONTROL

The AD9879 serial port is a flexible, synchronous serial communications port that allows easy interface to many industry-standard microcontrollers and microprocessors. The interface allows read/write access to all registers that configure the AD9879. Single or multiple byte transfers are supported. Also, the interface can be programmed to read words either MSB first or LSB first. The AD9879's serial interface port I/O can be configured to have one bidirectional I/O (SDIO) pin or two unidirectional I/O (SDIO/SDO) pins.

General Operation of the Serial Interface

There are two phases to a communication cycle with the AD9879. Phase 1 is the instruction cycle, which is the writing of an instruction byte into the AD9879, coincident with the first eight SCLK rising edges. The instruction byte provides the AD9879 serial port controller with information regarding the data transfer cycle, which is Phase 2 of the communication cycle. The Phase 1 instruction byte defines whether the upcoming data transfer is read or write, the number of bytes in the data transfer, and the starting register address for the first byte of the data transfer. The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the AD9879.

The eight remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the AD9879 and the system controller. Phase 2 of the communication cycle is a transfer of 1 to 4 data bytes as determined by the instruction byte. Normally, using one multibyte transfer is the preferred method. However, single byte data transfers are useful to reduce CPU overhead when register access requires one byte only. Registers change immediately upon writing to the last bit of each transfer byte.

Instruction Byte

The instruction byte contains the following information as shown below:

MSB							LSB
17	16	15	14	13	12	11	10
R/W	N1	N0	A4	A3	A2	A1	A0

The R/W bit of the instruction byte determines whether a read or a write data transfer will occur after the instruction byte write. Logic high indicates a read operation. Logic zero indicates a write operation. The N1:N0 bits determine the number of bytes to be transferred during the data transfer cycle. The bit decodes are shown in Table VI.

Table VI.

N1	N0	Description
0	0	Transfer 1 Byte
0	1	Transfer 2 Bytes
1	0	Transfer 3 Bytes
1	1	Transfer 4 Bytes

The Bits A4:A0 determine which register is accessed during the data transfer portion of the communications cycle. For multibyte transfers, this address is the starting byte address. The remaining register addresses are generated by the AD9879.

Serial Interface Port Pin Description

SCLK—Serial Clock. The serial clock pin is used to synchronize data transfers from the AD9879 and to run the serial port state machine. The maximum SCLK frequency is 15 MHz. Input data to the AD9879 is sampled on the rising edge of SCLK. Output data changes on the falling edge of SCLK.

$\overline{CS}$—Chip Select. Active low input starts and gates a communication cycle. It allows multiple devices to share a common serial port bus. The SDO and SDIO pins go to a high impedance state when $\overline{CS}$ is high. Chip select should stay low during the entire communication cycle.

SDIO—Serial Data I/O. Data is always written into the AD9879 on this pin. However, this pin can be used as a bidirectional data line. The configuration of this pin is controlled by Bit 7 of Register 0. The default is Logic 0, which configures the SDIO pin as unidirectional.

SDO—Serial Data Out. Data is read from this pin for protocols that use separate lines for transmitting and receiving data. In the case where the AD9879 operates in a single bidirectional I/O mode, this pin does not output data and is set to a high impedance state.

MSB/LSB Transfers

The AD9879 serial port can support both most significant bit (MSB) first or least significant bit (LSB) first data formats. This functionality is controlled by the LSB First Bit in Register 0. The default is MSB first.

When this bit is set active high, the AD9879 serial port is in LSB first format. In LSB first mode, the instruction byte and data bytes must be written from the least significant bit to the most significant bit. In LSB first mode, the serial port internal byte address generator increments for each byte of the multibyte communication cycle.

When this bit is set default low, the AD9879 serial port is in MSB first format. In MSB first mode, the instruction byte and data bytes must be written from the most significant bit to the least significant bit. In MSB first mode, the serial port internal byte address generator decrements for each byte of the multibyte communication cycle.

When incrementing from 0x1F, the address generator changes to 0x00. When decrementing from 0x00, the address generator changes to 0x1F.

Notes on Serial Port Operation

The AD9879 serial port configuration bits reside in Bits 6 and 7 of Register Address 00h. It is important to note that the configuration changes immediately upon writing to the last bit of the register. For multibyte transfers, writing to this register may occur during the middle of the communication cycle. Care must be taken to compensate for this new configuration for the remaining bytes of the current communication cycle.

The same considerations apply to setting the reset bit in Register Address 00h. All other registers are set to their default values, but the software reset does not affect the bits in Register Address 00h.

It is recommended to use only single byte transfers when changing serial port configurations or initiating a software reset.

A write to Bits 1, 2, and 3 of Address 00h with the same logic levels as Bits 7, 6, and 5 (bit pattern: XY1001YX binary) allows the user to reprogram a lost serial port configuration and to reset the registers to their default values. A second write to Address 00h with the RESET bit low and the serial port configuration as specified above (XY) reprograms the OSCIN multiplier setting. A changed f_{SYSCLK} frequency is stable after a maximum of tbd f_{MCLK} cycles (wake-up time).

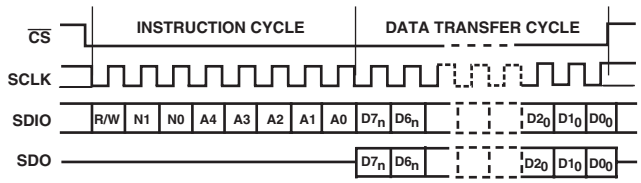


Figure 8a. Serial Register Interface Timing MSB First

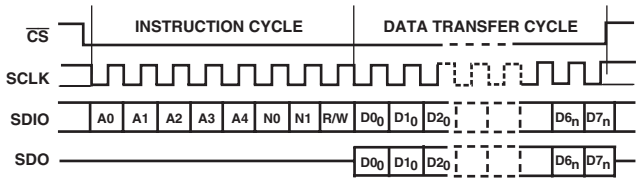


Figure 8b. Serial Register Interface Timing LSB First

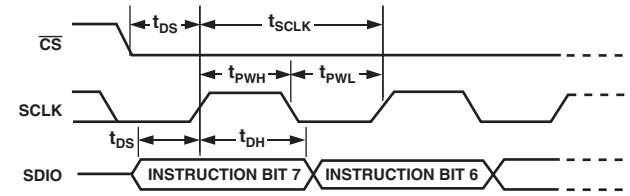


Figure 9. Timing Diagram for Register Write to AD9879

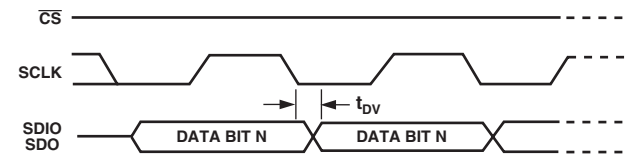


Figure 10. Timing Diagram for Register Read

TRANSMIT PATH (Tx)

Transmit Timing

The AD9879 provides a master clock MCLK and expects 6-bit multiplexed TxIQ data on each rising edge. Transmit symbols are framed with the TxSYNC input. TxSYNC high indicates the start of a transmit symbol. Four consecutive 6-bit data packages form a symbol (I MSB, I LSB, Q MSB, and Q LSB).

Data Assembler

The input data stream is representative complex data. Two 6-bit words form a 12-bit symbol component (in twos complement format). Four input samples are required to produce one I/Q data pair. The I/Q sample rate f_{IQCLK} at the input to the first half-band filter is a quarter of the input data rate f_{MCLK}. The I/Q sample rate f_{IQCLK} puts a bandwidth limit on the maximum transmit spectrum. This is the familiar Nyquist limit and is equal to one-half f_{IQCLK} that hereafter will be referred to as f_{NYQ}.

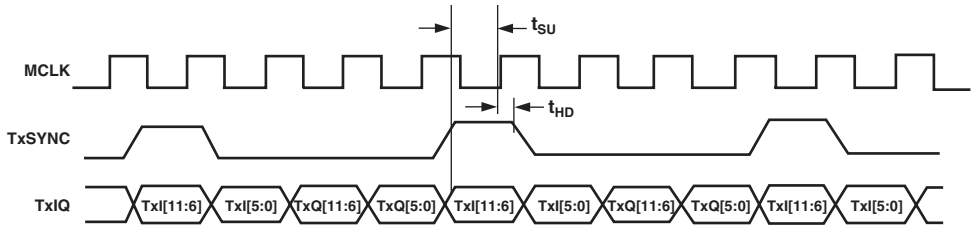


Figure 11. Timing Diagram for Register Read

Half-Band Filters (HBFs)

HBF 1 and HBF 2 are both interpolating filters, each of which doubles the sampling rate. Together, HBF 1 and HBF 2 have 26 taps and provide a factor-of-four increase in the sampling rate ($4 \times f_{IQCLK}$ or $8 \times f_{NYQ}$).

In relation to phase response, both HBFs are linear phase filters. As such, virtually no phase distortion is introduced within the pass band of the filters. This is an important feature as phase distortion is generally intolerable in a data transmission system.

Cascaded Integrator-COMB (CIC) Filter

The CIC filter is configured as a programmable interpolator and provides a sample rate increase by a factor of 4. The frequency response of the CIC filter is given by:

$$\left|H(f)\right| = \left[\left(\frac{1}{4}\right)\frac{1-e^{-j(2\pi f(4))}}{1-e^{j2\pi f}}\right]^3 = \left[\left(\frac{1}{4}\right)\frac{\sin(4\pi f)}{\sin(\pi f)}\right]^3$$

The frequency response in this form is such that f is scaled to the output sample rate of the CIC filter. That is, $f = 1$ corresponds to the frequency of the output sample rate of the CIC filter. H(f/R) will yield the frequency response with respect to the input sample of the CIC filter.

Combined Filter Response

The combined frequency response of HBF 1, HBF 2, and CIC puts a limit on the input signal bandwidth that can be propagated through the AD9879.

The usable bandwidth of the filter chain puts a limit on the maximum data rate that can be propagated through the AD9879. A look at the pass-band detail of the combined filter response (Figure 12 and Figure 13) indicates that in order to maintain an amplitude error of no more than 1 dB, we are restricted to signals having a bandwidth of no more than about 60% of f_{NYQ}. Thus, in order to keep the bandwidth of the data in the flat portion of the filter pass band, the user must oversample the baseband data by at least a factor of two prior to representing it to the AD9879. Note that without oversampling, the Nyquist bandwidth of the baseband data corresponds to the f_{NYQ}. As such, the upper end of the data bandwidth will suffer 6 dB or more of attenuation due to the frequency response of the digital filters. Furthermore, if the baseband data applied to the AD9879 has been pulse shaped, there is an additional concern. Typically, pulse shaping is applied to the baseband data via a filter having a raised cosine response. In such cases, an α value is used to modify the bandwidth of the data where the value of α is such that $0 < \alpha < 1$. A value of 0 causes the data bandwidth to correspond to the Nyquist bandwidth. A value of 1 causes the data bandwidth to be extended to twice the Nyquist bandwith. Thus, with 2× oversampling of the baseband data and $\alpha = 1$, the Nyquist bandwidth of the data will correspond with the I/Q Nyquist bandwidth. As stated earlier, this results in problems near the upper edge of the data bandwidth due to the frequency response of the filters. The maximum value of α that can be implemented is 0.45. This is because the data bandwidth becomes:

$$1/2\left(1+\alpha\right) f_{NYQ} = 0.725\, f_{NYQ}$$

which puts the data bandwidth at the extreme edge of the flat portion of the filter response.

If a particular application requires an α value between 0.45 and 1, then the user must oversample the baseband data by at least a factor of four.

The combined HB1, HB2, and CIC filter introduces, over the frequency range of the data to be transmitted, a worst-case droop of less than 0.2 dB.

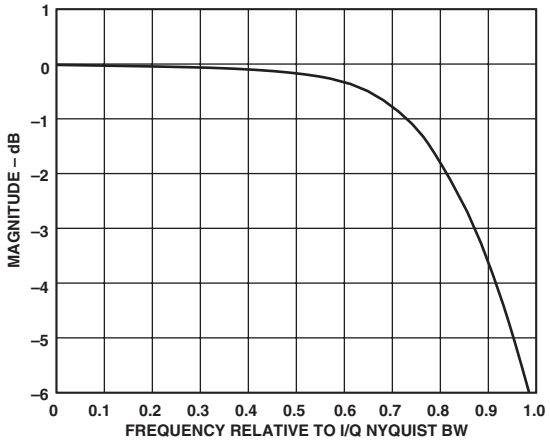


Figure 12. Cascaded Filter Pass-Band Detail (N = 4)

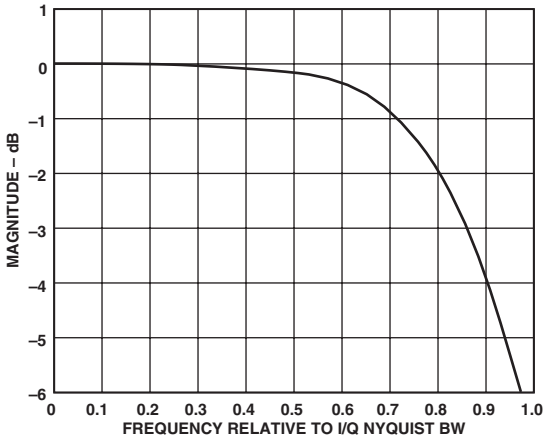


Figure 13. Cascaded Filter Pass-Band Detail (N = 3)

Tx Signal Level Considerations

The quadrature modulator itself introduces a maximum gain of 3 dB in signal level. To visualize this, assume that both the I data and Q data are fixed at the maximum possible digital value, *x*. Then the output of the modulator, *z* is:

$$z = \left[x\ cos(\omega t) - x\ sin(\omega t)\right]$$

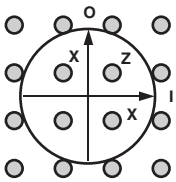


Figure 14. 16-Quadrature Modulation

It can be shown that $|z|$ assumes a maximum value of $|z| = (x^2 + x^2) = \sqrt{2}$ (a gain of +3 dB). However, if the same number of bits were used to represent the $|z|$ values, as is used to represent the *x* values, an overflow would occur. To prevent this possibility, an effective –3 dB attenuation is internally implemented on the I and Q data path:

$$\left(|z| = \sqrt{(1/2 + 1/2)} = x\right)$$

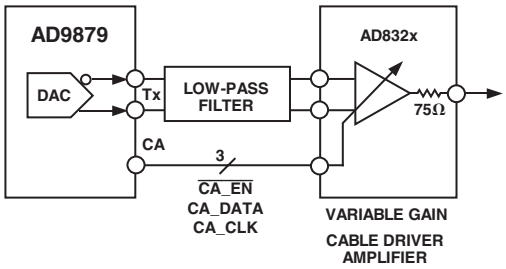


Figure 15. 16-Quadrature Modulation

The following example assumes an PK/rms level of 10 dB:

$$Maximum\ Symbol\ Component\ Input\ Value = \pm\left(2047\ LSBs - 0.2\ dB\right) = \pm 2000\ LSBs$$

$$Maximum\ Complex\ Input\ RMS\ Value = 2000\ LSBs \pm 6\ dB - Pk/rms\ \left(dB\right) = 1265\ LSBs\ rms$$

The maximum complex input rms value calculation uses both I and Q symbol components that add a factor of 2 (= 6 dB) to the formula. Table VII shows typical I-Q input test signals with amplitude levels related to 12-bit full scale (FS).

Tx Throughput and Latency

Data inputs effect the output fairly quickly but remain effective due to AD9879's filter characteristics. Data transmit latency through the AD9879 is easiest to describe in terms of f_{SYSCLK} clock cycles (4 f_{MCLK}). The numbers quoted are when an effect is first seen after an input value change.

Latency of I/Q data entering the data assembler (AD9879 input) to the DAC output is 119 f_{SYSCLK} clock cycles (29.75 f_{MCLK} cycles). DC values applied to the data assembler input will take up to 176 f_{SYSCLK} clock cycles (44 f_{MCLK} cycles) to propagate and settle at the DAC output.

Frequency hopping is accomplished via changing the PROFILE input pin. The time required to switch from one frequency to another is less than 232 f_{SYSCLK} cycles (58.5 f_{MCLK} cycles).

D/A Converter

A 12-bit digital-to-analog converter (DAC) is used to convert the digitally processed waveform into an analog signal. The worst-case spurious signals due to the DAC are the harmonics of the fundamental signal and their aliases (please see the Analog Devices DDS Tutorial at: www.analog.com/dds). The conversion process will produce aliased components of the fundamental signal at $n \times f_{SYSCLK} \pm f_{CARRIER}$ (n = 1, 2, 3). These are typically filtered with an external RLC filter at the DAC output. It is important for this analog filter to have a sufficiently flat gain and linear phase response across the bandwidth of interest so as to avoid modulation impairments. A relatively inexpensive seventh order elliptical low-pass filter is sufficient to suppress the aliased components for HFC network applications.

The AD9879 provides true and complement current outputs. The full-scale output current is set by the R_{SET} resistor at Pin 49 and the DAC Gain register. Assuming maximum DAC gain, the value of R_{SET} for a particular full-scale I_{OUT} is determined using the following equation:

$$R_{SET} = 32 V_{DACRSET} / I_{OUT} = 39.4 / I_{OUT}$$

For example, if a full-scale output current of 20 mA is desired, then R_{SET} = (39.4/0.02) Ω, or approximately 2 kΩ.

The following equation calculates the full-scale output current including the programmable DAC gain control.

$$I_{OUT} = [39.4 / R_{SET}] \times 10\text{^}((-7.5 + 0.5\ NGAIN) / 20)$$

where N_{GAIN} is the value of DAC Fine Gain Control[3:0].

Table VII. I–Q Input Test Signals

Analog Output	Digital Input	Input Level	Modulator Output Level
Single Tone (f_C – f)	I = cos(f) Q = cos(f + 90°) = –sin(f)	FS – 0.2 dB FS – 0.2 dB	FS – 3.0 dB
Single Tone (f_C + f)	I = cos(f) Q = cos(f + 270°) = +sin(f)	FS – 0.2 dB FS – 0.2 dB	FS – 3.0 dB
Dual Tone (f_C ± f)	I = cos(f) Q = cos(f + 180°) = –cos(f) or Q = +cos(f)	FS – 0.2 dB FS – 0.2 dB	FS

The full-scale output current range of the AD9879 is 4 mA–20 mA. Full-scale output currents outside of this range will degrade SFDR performance. SFDR is also slightly affected by output matching, that is, the two outputs should be terminated equally for best SFDR performance. The output load should be located as close as possible to the AD9879 package to minimize stray capacitance and inductance. The load may be a simple resistor to ground, an op amp current-to-voltage converter, or a transformer-coupled circuit. It is best not to attempt to directly drive highly reactive loads (such as an LC filter). Driving an LC filter without a transformer requires that the filter be doubly terminated for best performance, that is, the filter input and output should both be resistively terminated with the appropriate values. The parallel combination of the two terminations will determine the load that the AD9879 will see for signals within the filter pass band. For example, a 50 Ω terminated input/output low-pass filter will look like a 25 Ω load to the AD9879. The output compliance voltage of the AD9879 is –0.5 V to +1.5 V. Any signal developed at the DAC output should not exceed +1.5 V, otherwise signal distortion will result. Furthermore, the signal may extend below ground as much as 0.5 V without damage or signal distortion. The AD9879 true and complement outputs can be differentially combined for common-mode rejection using a broadband 1:1 transformer. Using a grounded center tap results in signals at the AD9879 DAC output pins that are symmetrical about ground. As previously mentioned, by differentially combining the two signals, the user can provide some degree of common-mode signal rejection. A differential combiner might consist of a transformer or an operational amplifier. The object is to combine or amplify only the difference between two signals and to reject any common, usually undesirable, characteristic, such as 60 Hz hum or clock feedthrough that is equally present on both individual signals.

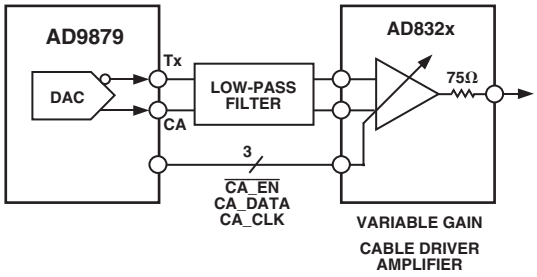


Figure 16. Cable Amplifier Connection

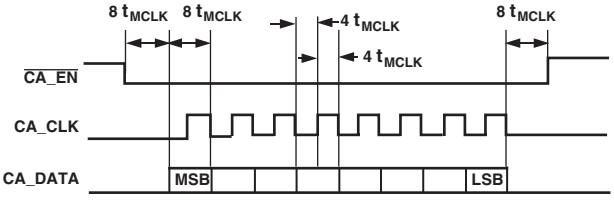


Figure 17. Cable Amplifier Interface Timing

Connecting the AD9879 true and complement outputs to the differential inputs of the gain programmable cable drivers AD8321/AD8323 or AD8322/AD8327 provides an optimized solution for the standard compliant cable modem upstream channel. The cable driver's gain can be programmed through a direct 3-wire interface using the AD9879's profile registers.

PROGRAMMING THE AD8321/AD8323 OR AD8323/AD8327 CABLE DRIVER AMPLIFIER GAIN CONTROL

Programming the gain of the AD832x family of cable driver amplifiers can be accomplished via the AD9879 cable amplifier control interface. Four 8-bit registers within the AD9879 (one per profile) store the gain value to be written to the serial 3-wire port. Typically, either the AD8321/AD8323 or AD8222/AD8227 variable gain cable amplifiers are connected to the chip's 3-wire cable amplifier interface. The Tx Gain Control Select bit in Register 0Fh changes the interpretation of the bits in Register 13h, 17h, 1Bh, and 1Fh. See Cable Driver Gain Control Register description.

Data transfers to the gain programmable cable driver amplifier are initiated by four conditions including:

1. Power-up and Hardware Reset—Upon initial power up and every hardware reset, the AD9879 clears the contents of the gain control registers to 0, which defines the lowest gain setting of the AD832x. Thus, the AD9879 writes all 0s out of the 3-wire cable amplifier control interface.
2. Software Reset—Writing a 1 to Bit 5 of Address 00h initiates a software reset. On a software reset, the AD9879 clears the contents of the gain control registers to 0 for the lowest gain and sets the profile select to 0. The AD9879 writes all 0s out of the 3-wire cable amplifier control interface if the gain was on a different setting (different from 0) before.
3. Change in Profile Selection—The AD9879 sample the PROFILE input pin together with the two Profile Select Bits and writes to the AD832x gain control registers when a change in profile and gain is determined. The data written to the cable driver amplifier comes from the AD9879 gain control register associated with the current profile.
4. Write to AD9879 Cable Driver Amplifier Control Registers—The AD9879 will write gain control data associated with the current profile to the AD832x whenever the selected AD9879 cable driver amplifier gain setting is changed.

Once a new stable gain value has been detected (48 MCLK to 64 MCLK cycles after initiation) data write starts with CA_EN going low. The AD9879 will always finish a write sequence to the cable driver amplifier once it is started. The logic controlling data transfers to the cable driver amplifier uses up to 200 MCLK cycles and has been designed to prevent erroneous write cycles from ever occurring.

RECEIVE PATH (Rx)

IF10 and IF12 ADC Operation

The IF10 and IF12 ADCs have a common architecture and share many of the same characteristics from an applications standpoint. Most of the information in the section below will be applicable to both IF ADCs. Differences, where they exist, will be highlighted.

Input Signal Range and Digital Output Codes

The IF ADCs have differential analog inputs labelled IF+ and IF–. The signal input, V_{AIN}, is the voltage difference between the two input pins, $V_{AIN} = V_{IF+} – V_{IF–}$. The full-scale input voltage range is determined by the internal reference voltages, REFT and REFB, which define the top and bottom of the scale. The peak input voltage to the ADC is the difference between REFT and REFB which is 1 V_{PD}. This results in the ADC full-scale input voltage range of 2 V_{PPD}. The digital output code is straight binary and is illustrated in Table VIII.

Table VIII.

IF[11:0]	Input Signal Voltage
111...111	V_{AIN} >= +1.0 V
111...111	V_{AIN} = +1.0 – (1 LSB) V
111...110	V_{AIN} = +1.0 – (2 LSB) V
...	
100...001	V_{AIN} = +1 LSB V
100...000	V_{AIN} = 0.0 V
011...111	V_{AIN} = –1 LSB V
...	
000...001	V_{AIN} = –1.0 + (2 LSB) V
000...000	V_{AIN} = –1.0 V
000...000	V_{AIN} < –1.0 V

The IF10 ADC digital output code occupies the 10 most significant bits of the Rx digital output port (IF[11:2]). The output codes clamp to the top or the bottom of the scale when the inputs are overdriven.

Driving the Input

The IF ADCs have differential switched capacitor sample-and-hold amplifier (SHA) inputs. The nominal differential input impedance is 4.0 kΩ||3 pF. This impedance can be used as the effective termination impedance when calculating filter transfer characteristics and voltage signal attenuation from non-zero source impedances. It should be noted however that for best performance additional requirements must be met by the signal source. The SHA has input capacitors that must be recharged each time the input is sampled. This results in a dynamic input current at the device input. This demands that the source has low (<50 V) output impedance at frequencies up to the ADC sampling frequency. Also, the source must have settling to better than 0.1% in <1/2 ADC CLK period.

Another consideration for getting the best performance from the ADC inputs is the dc biasing of the input signal. Ideally, the signal should be biased to a dc level equal to the midpoint of the ADC reference voltages, REFT12 and REFB12. Nominally, this level will be 1.2 V. When ac-coupled, the ADC inputs will self-bias to this voltage and requires no additional input circuitry.

Figure 20 illustrates a recommended circuit that eases the burden on the signal source by isolating its output from the ADC input. The 33 Ω series termination resistors isolate the amplifier outputs from any capacitive load, which typically improves settling time. The series capacitors provide ac signal coupling which ensures that the ADC inputs operate at the optimal dc bias voltage. The shunt capacitor sources the dynamic currents required to charge the SHA input capacitors, removing this requirement from the ADC buffer. The values of CC and CS should be calculated to get the correct HPF and LPF corner frequencies.

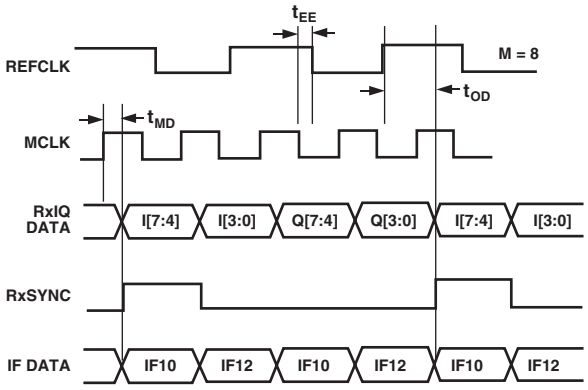


Figure 18. Rx Port Timing (Default Mode: Multiplexed IF ADC Data)

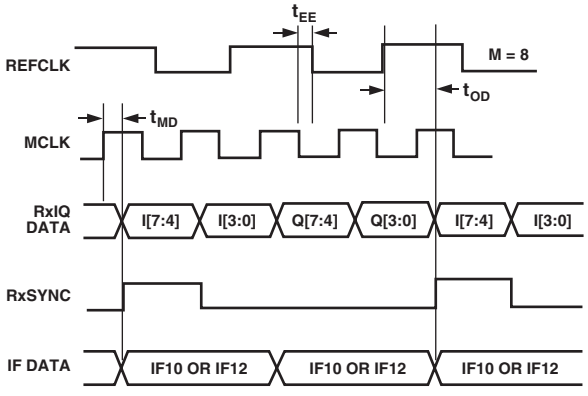


Figure 19. Rx Port Timing (Nonmultiplexed Data)

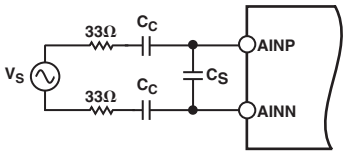


Figure 20. Simple ADC Drive Configuration

PCB DESIGN CONSIDERATIONS

Although the AD9879 is a mixed-signal device, the part should be treated as an analog component. The digital circuitry on-chip has been specially designed to minimize the impact that the digital switching noise will have on the operation of the analog circuits. Following the power, grounding, and layout recommendations in this section will help the user get the best performance from the MxFE.

Component Placement

If the three following guidelines of component placement are followed, chances for getting the best performance from the MxFE are greatly increased. First, manage the path of return currents flowing in the ground plane so that high frequency switching currents from the digital circuits do not flow on the ground plane under the MxFE or analog circuits. Second, keep noisy digital signal paths and sensitive receive signal paths as short as possible. Third, keep digital (noise generating) and analog (noise susceptible) circuits as far away from each other as possible.

In order to best manage the return currents, pure digital circuits that generate high switching currents should be closest to the power supply entry. This will keep the highest frequency return current paths short, and prevent them from traveling over the sensitive MxFE and analog portions of the ground plane. Also, these circuits should be generously bypassed at each device which will further reduce the high frequency ground currents. The MxFE should be placed adjacent to the digital circuits, such that the ground return currents from the digital sections will not flow in the ground plane under the MxFE. The analog circuits should be placed furthest from the power supply.

The AD9879 has several pins which are used to decouple sensitive internal nodes. These pins are REFIO, REFB10, REFT10, REFB12, and REFT12. The decoupling capacitors connected to these points should have low ESR and ESL. These capacitors should be placed as close to the MxFE as possible and be connected directly to the analog ground plane.

The resistor connected to the FSADJ pin and the RC network connected to the PLLFILT pin should also be placed close to the device and connected directly to the analog ground plane.

Power Planes and Decoupling

The AD9879 evaluation board demonstrates a good power supply distribution and decoupling strategy. The board has four layers; two signal layers, one ground plane and one power plane. The power plane is split into a 3 VDD section which is used for the 3 V digital logic circuits, a DVDD section that is used to supply the digital supply pins of the AD9879, an AVDD section that is used to supply the analog supply pins of the AD9879, and a VANLG section that supplies the higher voltage analog components on the board. The 3 VDD section will typically have the highest frequency currents on the power plane and should be kept the furthest from the MxFE and analog sections of the board.

The DVDD portion of the plane brings the current used to power the digital portion of the MxFE to the device. This should be treated similar to the 3VDD power plane and be kept from going underneath the MxFE or analog components. The MxFE should largely sit above the AVDD portion of the power plane.

The AVDD and DVDD power planes may be fed from the same low noise voltage source; however, they should be decoupled from each other to prevent the noise generated in the DVDD portion of the MxFE from corrupting the AVDD supply. This can be done by using ferrite beads between the voltage source and DVDD and between the source and AVDD. Both DVDD and AVDD should have a low ESR, bulk decoupling capacitor on the MxFE side of the ferrite as well as a low ESR, ESL decoupling capacitors on each supply pin (i.e., the AD9879 requires 17 power supply decoupling caps). The decoupling caps should be placed as close to the MxFE supply pins as possible. An example of the proper decoupling is shown in the AD9875 evaluation board schematic.

Ground Planes

In general, if the component placing guidelines discussed earlier can be implemented, it is best to have at least one continuous ground plane for the entire board. All ground connections should be made as short as possible. This will result in the lowest impedance return paths and the quietest ground connections.

If the components cannot be placed in a manner that would keep the high frequency ground currents from traversing under the MxFE and analog components, it may be necessary to put current steering channels into the ground plane to route the high frequency currents around these sensitive areas. These current steering channels should be made only when and where necessary.

Signal Routing

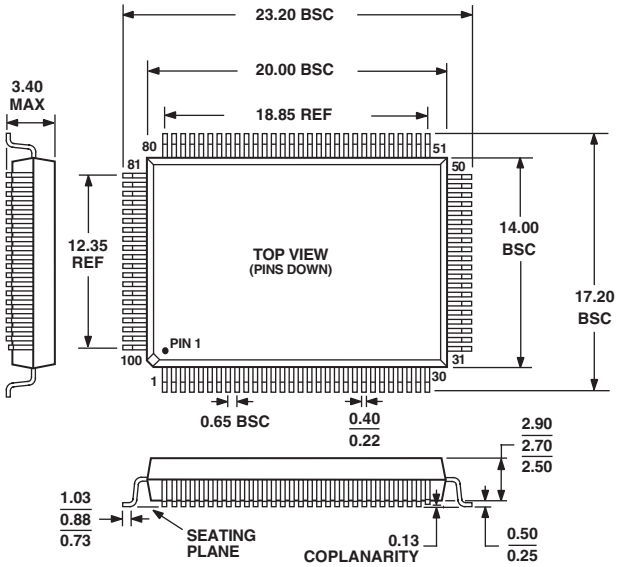
The digital Rx and Tx signal paths should be kept as short as possible. Also, the impedance of these traces should have a controlled impedance of about 50 Ω. This will prevent poor signal integrity and the high currents that can occur during undershoot or overshoot caused by ringing. If the signal traces cannot be kept shorter than about 1.5 inches, then series termination resistors (33 Ω to 47 Ω) should be placed close to all signal sources. It is a good idea to series terminate all clock signals at their source regardless of trace length.

The receive (I in, Q in, and RF in) signals are the most sensitive signals on the entire board. Careful routing of these signals is essential for good receive path performance. The Rx+/– signals form a differential pair and should be routed together as a pair. By keeping the traces adjacent to each other, noise coupled onto the signals will appear as common mode and will be largely rejected by the MxFE receive input. Keeping the driving point impedance of the receive signal low and placing any low-pass filtering of the signals close to the MxFE will further reduce the possibility of noise corrupting these signals.

OUTLINE DIMENSIONS

100-Lead Plastic Quad Flatpack (MQFP)
(S-100C)

Dimensions shown in millimeters



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