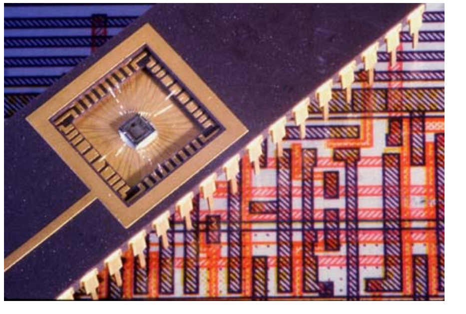
ENIAC

From Vacuum Tubes to Microchip

History, Operation and Reconstruction in VLSI



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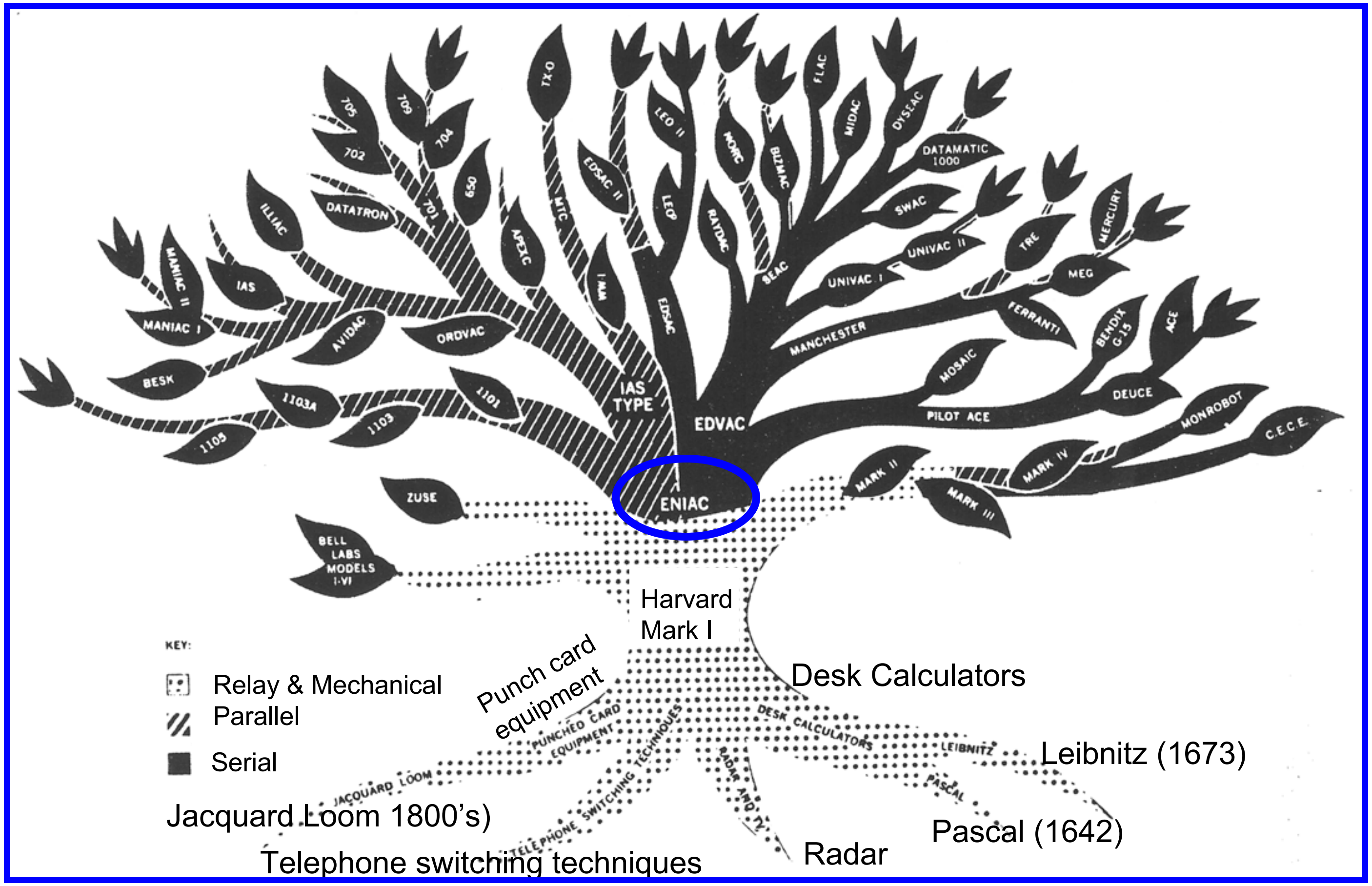
Overview

- Introduction
- Brief History
- ENIAC's Architectural Overview
- Operation of ENIAC's units
- Programming Exercise
- ENIAC-on-a-Chip Implementation
- Summary

ENIAC

- **E**lectronic **N**umerical **I**ntegrator **a**nd **C**omputer
- Often considered as a milestone in computer development:
  - First **digital**
  - **Electronic** and
  - **General purpose** computer
- Proved that electronic computing was not only possible but also advantageous.

ENIAC and its Family Tree



Bell and Newell "family tree", M. Williams.

A Brief Historical Overview

Background: World Ware II

- Ballistic Research Laboratory of the U.S. Army was preparing **firing tables** for the various new weapons under development.
- These computations were so time-consuming that the labs could not keep up fast enough.
- Asked the help of the Moore School at the Univ. of Pennsylvania
  - Human computers
  - Differential analyzer

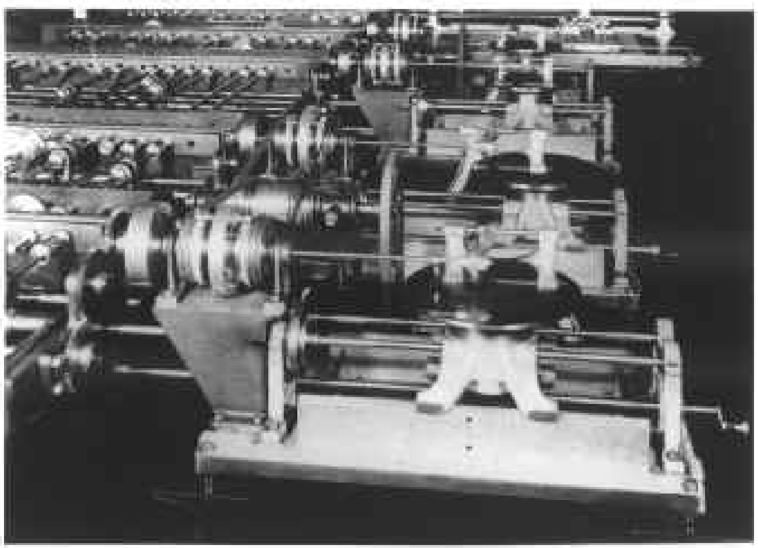
STANDARD CONDITIONS	
WEATHER	
1	AIR TEMPERATURE 100 PERCENT (59°F)
2	AIR DENSITY 100 PERCENT (1,225 gm/m^3)
3	NO WIND
POSITION	
1	GUN, TARGET, AND MDP AT SAME ALTITUDE
2	ACCURATE RANGE
3	NO ROTATION OF THE EARTH
MATERIAL	
1	STANDARD WEAPON, PROJECTILE, AND FUZE
2	PROPELLANT TEMPERATURE (70°F)
3	LEVEL TRUNNIONS AND PRECISION SETTINGS
4	FIRING TABLE MUZZLE VELOCITY
5	NO DRIFT
LEGEND:	gm/m^3 – grams per cubic meter

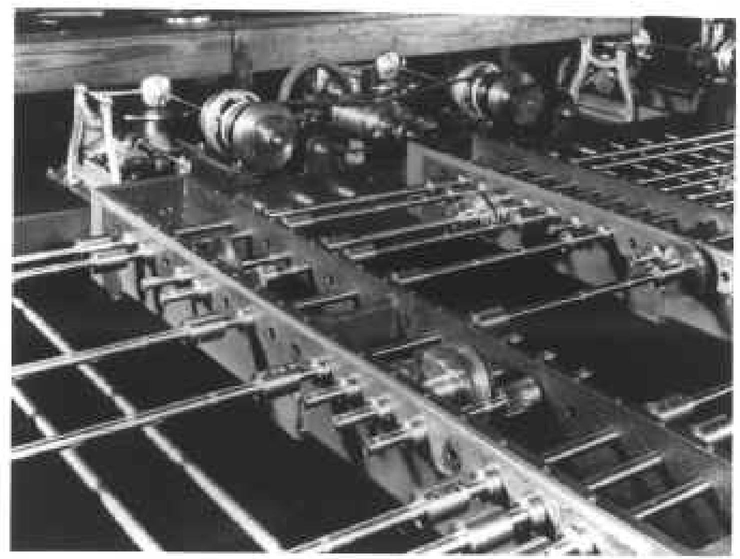
Human computers

- It took a human **40 hr**. for one trajectory

Differential Analyzer

- Was the fastest machine of its time!
- It took still **30 min**./trajectory (one month per table)





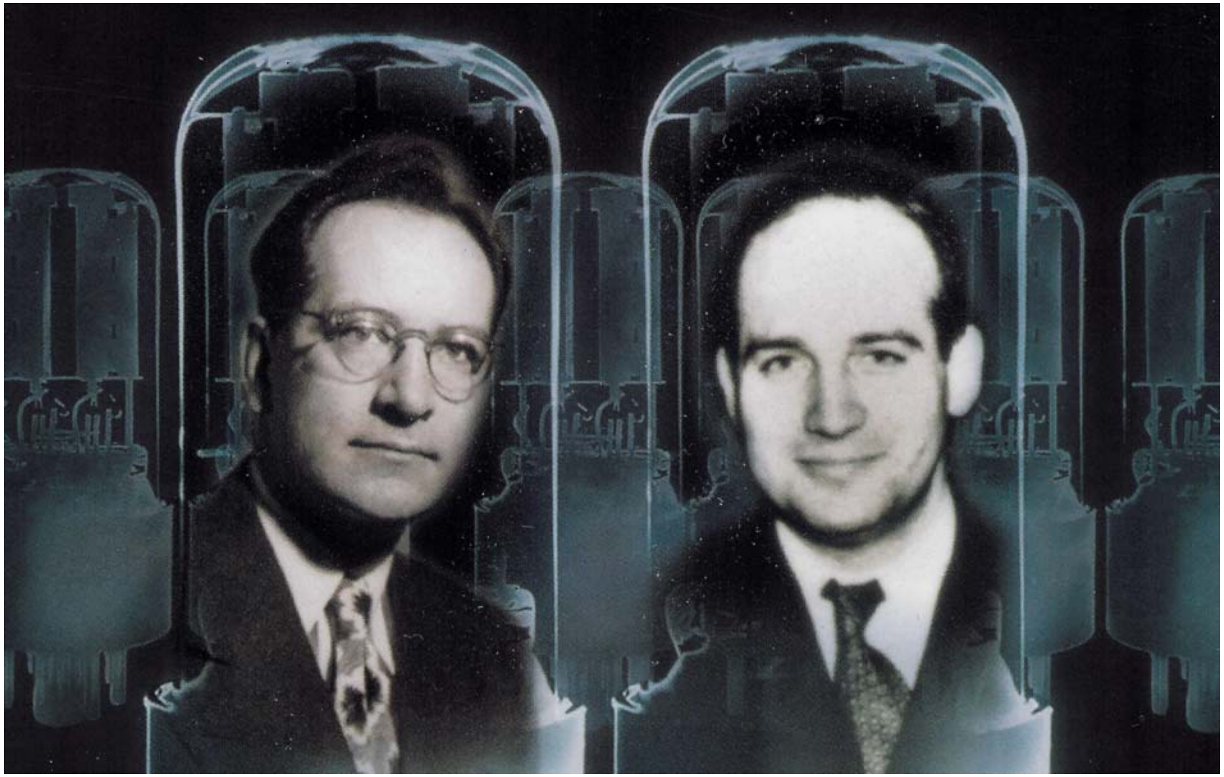
(Source: http://web.mit.edu/mindell/www/analyzer.htm

Idea of ENIAC was born

- Mauchly (36)and Eckert (24) proposed to build an Electronic Machine, using vacuum tubes.
- Pretty radical idea.
- Many skeptics doubted the feasibility

- ENIAC was built in the period from May 1943 to November 1945.

Inventors: P. Eckert and J. Mauchly



(Source: "ENIAC - The Triumphs and Tragedies of the Worlds First Computer", S. McCartney, Walker & Co, New York, 1999)

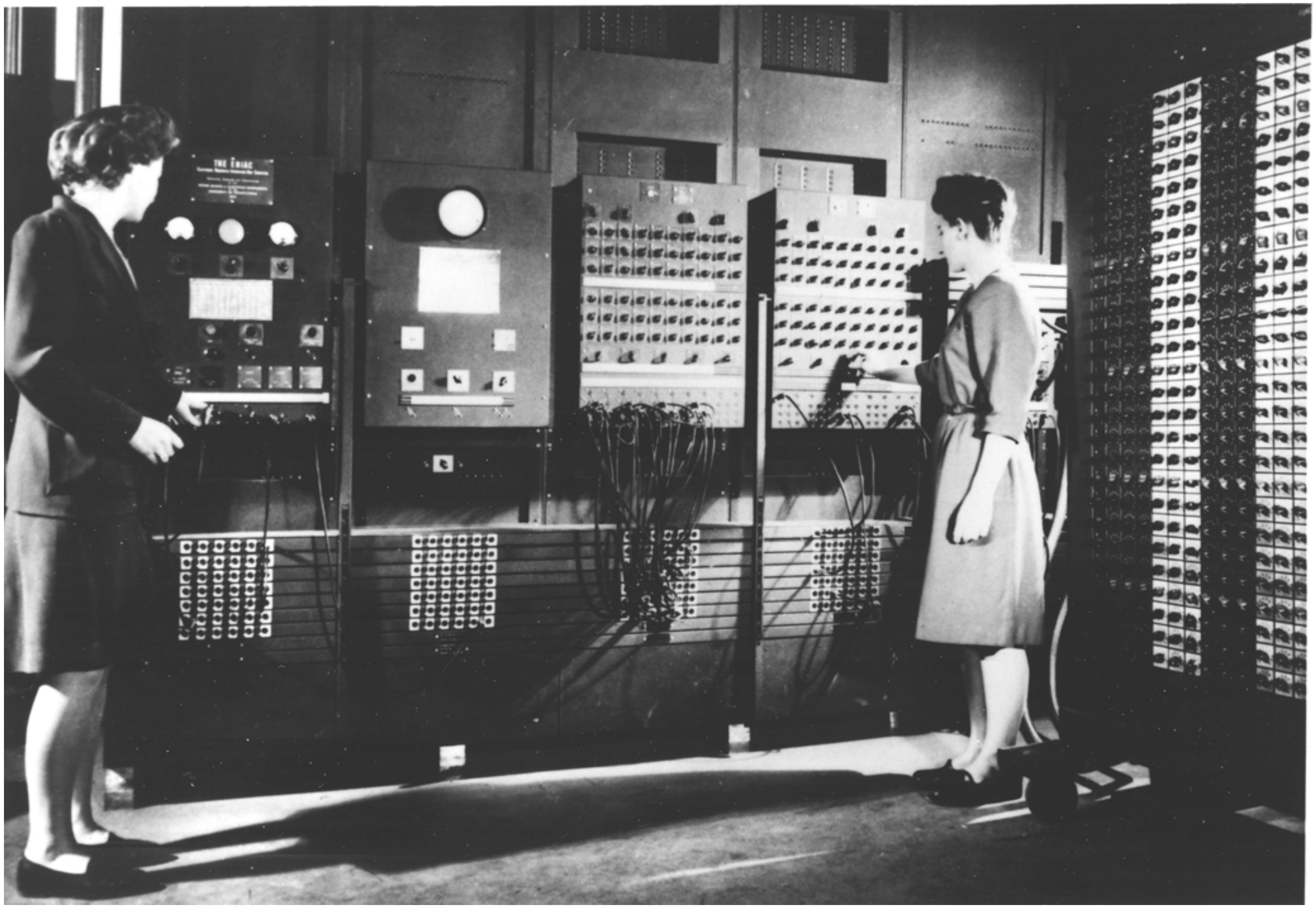
Valentines day of 1946

- Eniac was unveiled to the public on 14 Feb. 1946
- Stunned the scientific, military and industrial community:
  – about **1000** x faster than any other machine
  – made it possible to do more calculation than was done in all of history up to that point.
- Captured the imagination of the public

ENIAC - a truly large scale machine

(Courtesy, Univ. of Pennsylvania)

ENIAC close-up



(Courtesy, Univ. of Pennsylvania)

ENIAC - a truly large scale machine

- Occupied 1800 sq. ft. (room of 10m x 17m)
- 30 tons
- 40 panels in U-shape (80 ft long)
- 3 portable function tables
- card reader and card punch
- 174,000 Watts
- cost: $486,000 in 1946

New York Times, 14th February 1946

- "*... an amazing machine which applies electronic speeds for the first time to mathematical tasks hitherto too difficult and cumbersome for solutions ...*

  Leaders who saw the device in action for the first time heralded it as a tool with which to begin to rebuild scientific affairs on a new foundation."

Newsweek Magazine, 18 Feb. '46

- ... *The first problems put to Eniac was a nuclear-physics calculation that would require* ***100 man-years*** *of work by a trained computer. The electronic device solved it in two weeks of which* ***two hours*** *were used for the actual electronic computing and the remaining time for operating details and review of results."*

Predicting the future

- Thomas Watson of IBM:
  "... a world market of about 5 computers."

- Howard Aiken of Harvard University:
  "There will never be enough work for more than two of these programs."

Skeptics were proven wrong

- Innovations in manufacturing:
  - Use a small number of elements
  - Interchangeable modules: plug-ins
- Overcome reliability problems:
  - burn-in tubes and pre-select
  - operate tubes well below specs
  - use tubes only as on-off elements
  - careful circuit design
- Down time: 2-3 hr. per week

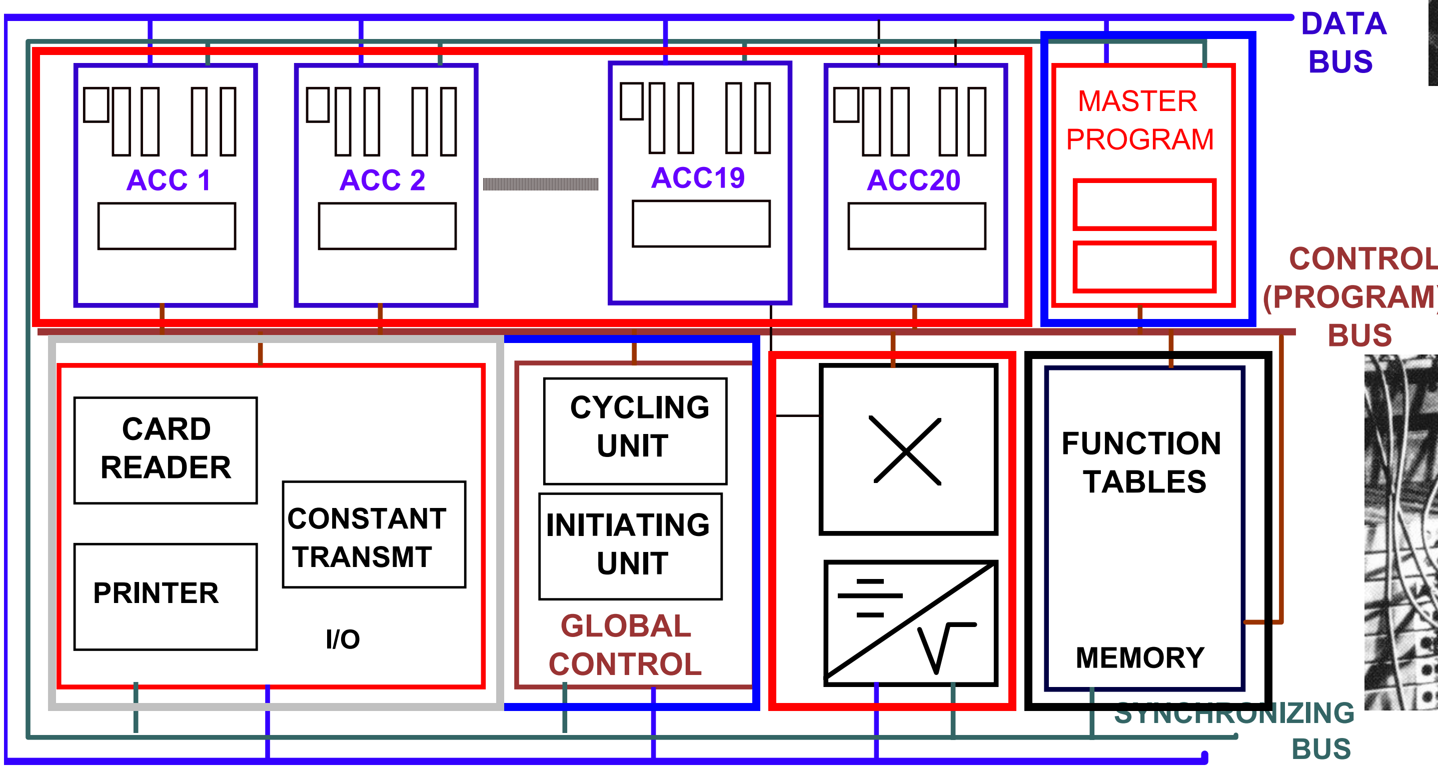
Architectural Overview

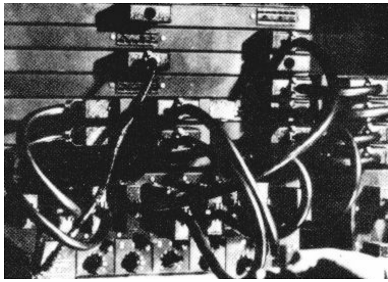
Architectural Overview

- Digital machine
- Conceived as an electronic analog of a mechanical adding machine
- The inventors wanted to make ENIAC more flexible than mechanical adding machines:
  - programmed sequence of operations
  - storing intermediate results
  - nested loops
  - **conditional branching**
  - reading and printing numbers

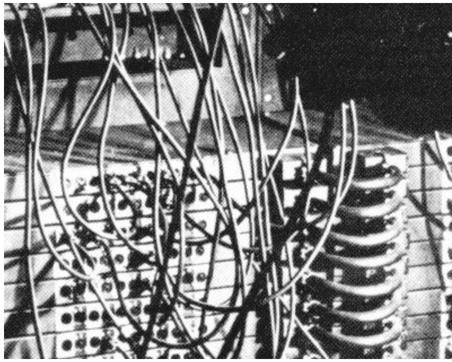
Functional Block Diagram

- ENIAC: Dataflow Machine
- Accumulator based





Digit trunks



Program trunks

Design decisions

- ENIAC was built under time pressure
- Number representation: binary vs. decimal
  - Decimal numbers requires fewer vacuum tubes (280 vs. 450)
- Number transmission: static vs. dynamic
  - Few interconnections for dynamic (pulse) transmission

Number representation

- Decimal: 10 digits and Sign
- Fixed point
- Double precision possible: 20 digits
- Fewer than 10 digits possible
- Negative numbers: 10's complement

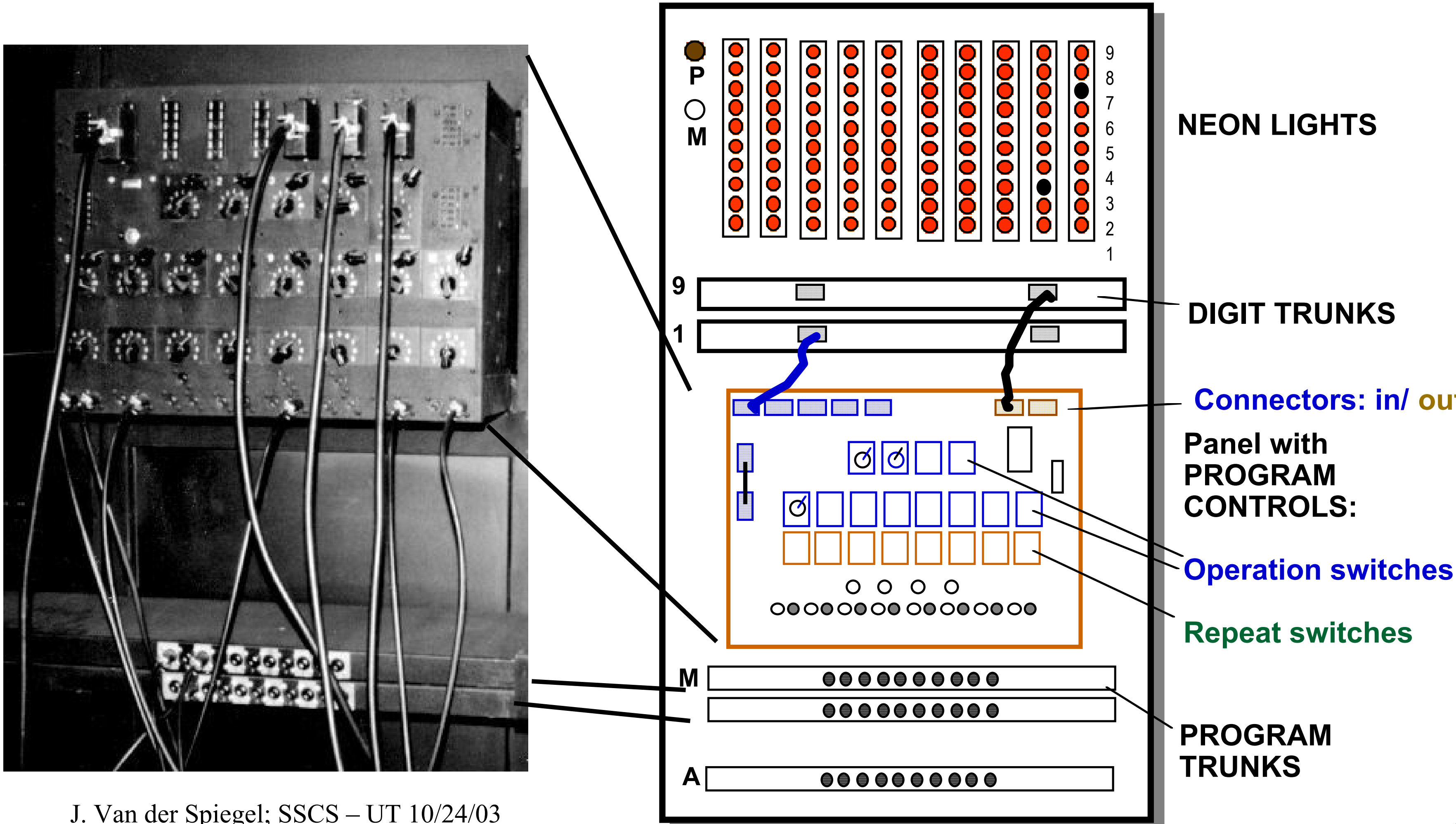
$$-N = 10^{10} - N = [(10^{10} - 1) - N + 1]$$

$$-124 = M + 9\ 999\ 999\ 876$$

Communications: pulse transmission

- Numbers transmitted as pulses:
  - fewer connections than static transmission
  - fewer vacuum tubes
- Pulses occurred at rate of 100 kHz
- All 10 digits were transmitted in parallel
- Static transmission: for dedicated connections

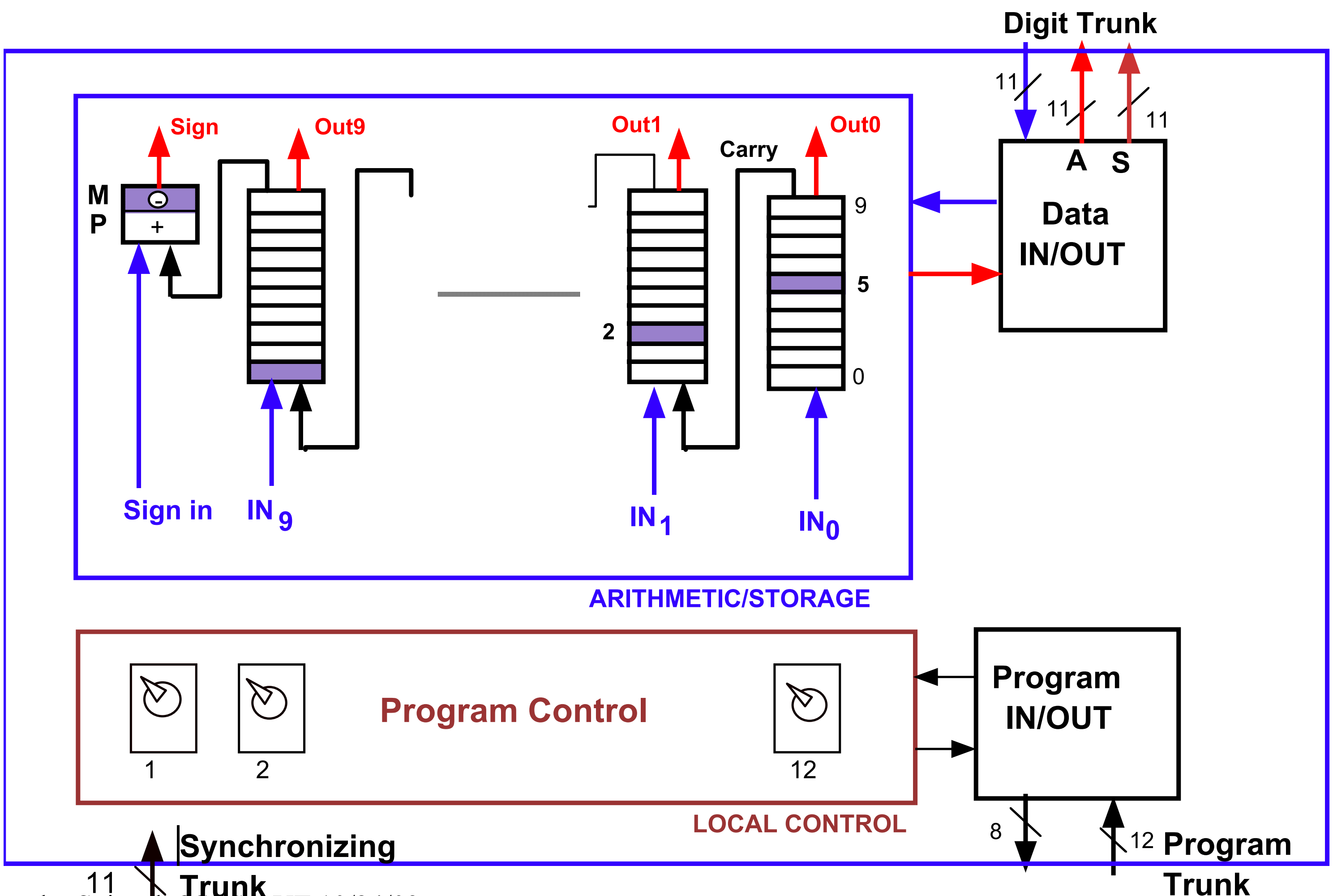
Accumulator's front panel



Accumulator program controls

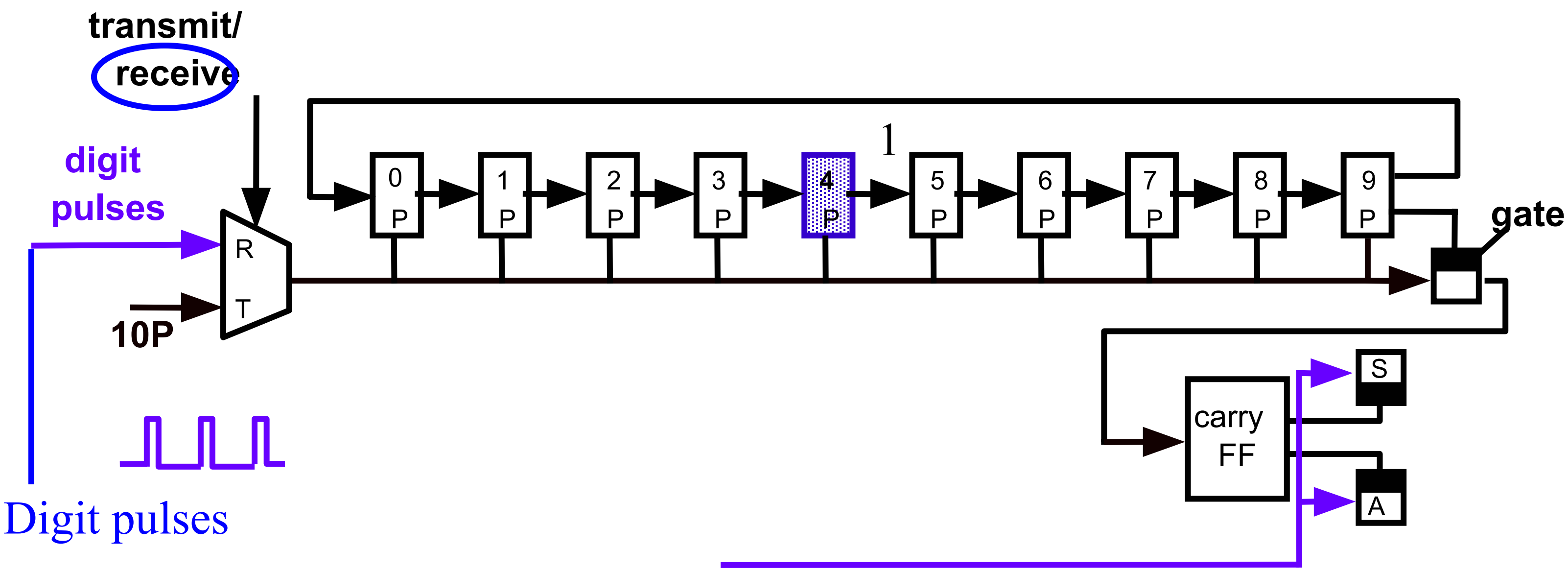
- **Local Program Control**: *Operation switches* and *Repeat switches*
- *Operation switches: 5 possible operations*
  - receive (on one of 5 input channels α, β, γ, δ, ε)
  - transmit additively, subtractively, or both (A, S, AS)
  - do nothing
- *Repeat switches*: up to 9x.

Accumulator Block Diagram



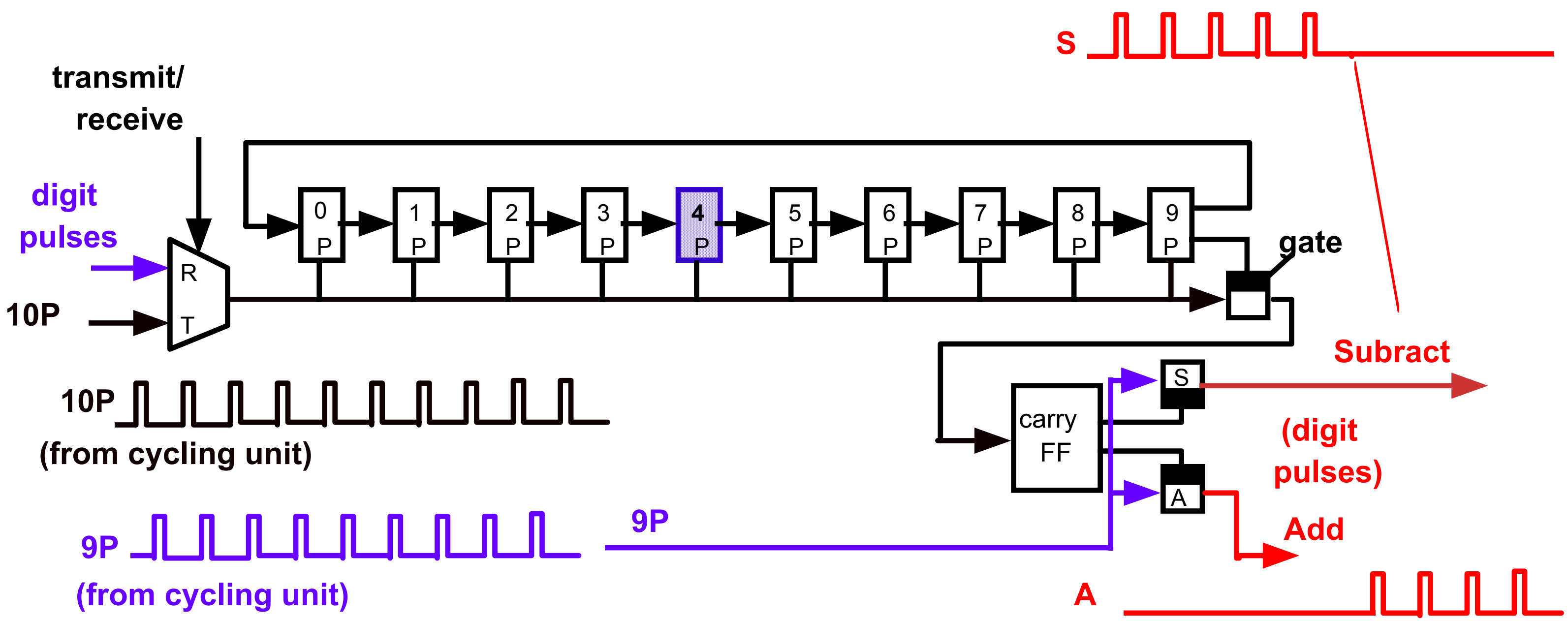
Receiving numbers (adding)

- Number stored "**4**"
- Add number 3; sum 7
- Receives 3 digit pulses



Number transmission

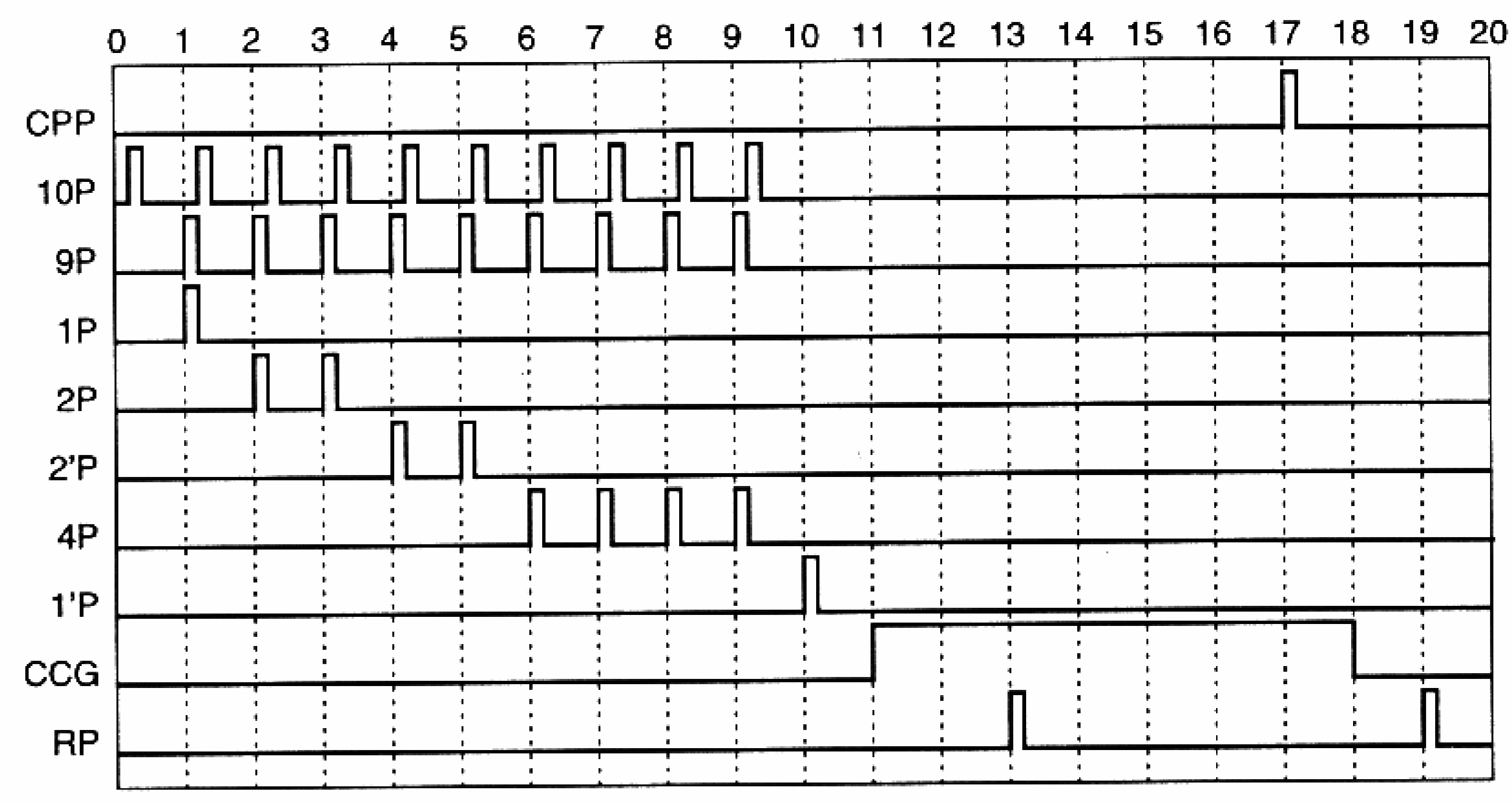
- Transmit number “4”
- Simplified diagram of decade counter



Cycling Unit - keeping ENIAC synchronized

- Provides fundamental pulses
  - rate of 100 kHz
  - one addition cycle: 20 pulse units (0.2msec)
- Three modes
  - Continuous
  - One addition mode
  - One pulse mode

Cycling Unit - pulse trains



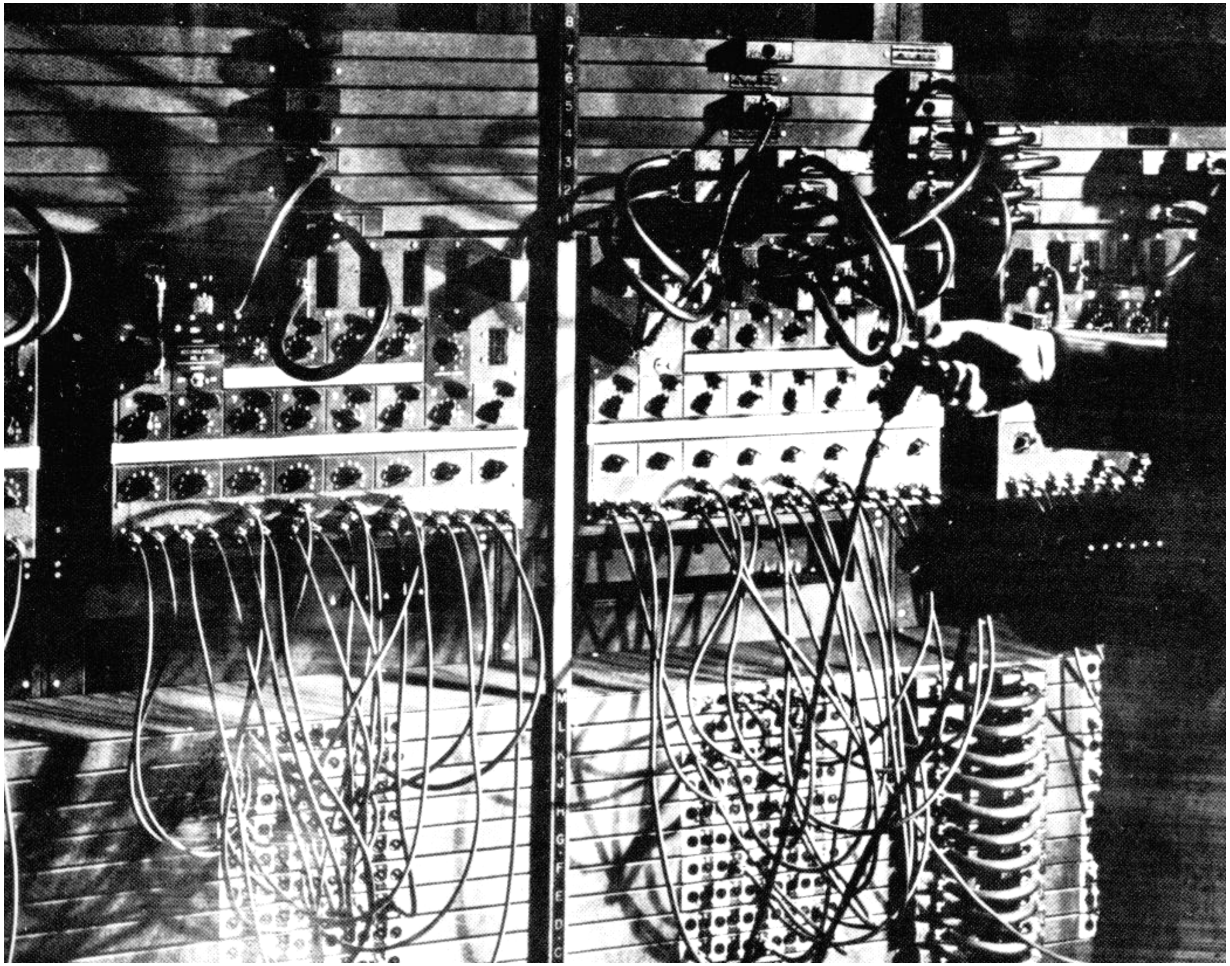
Programming … a time-consuming task!

- Complex problems could take 1-2 months to set up a program
- Set up the machine: 1-2 days
- Debugging: 1 week

Programming of ENIAC

- Specify type of operations by setting the Operation and Repeat switches of the local programs
- Specify the temporal sequence by connecting the program input and output terminals
- Connecting digit trunks

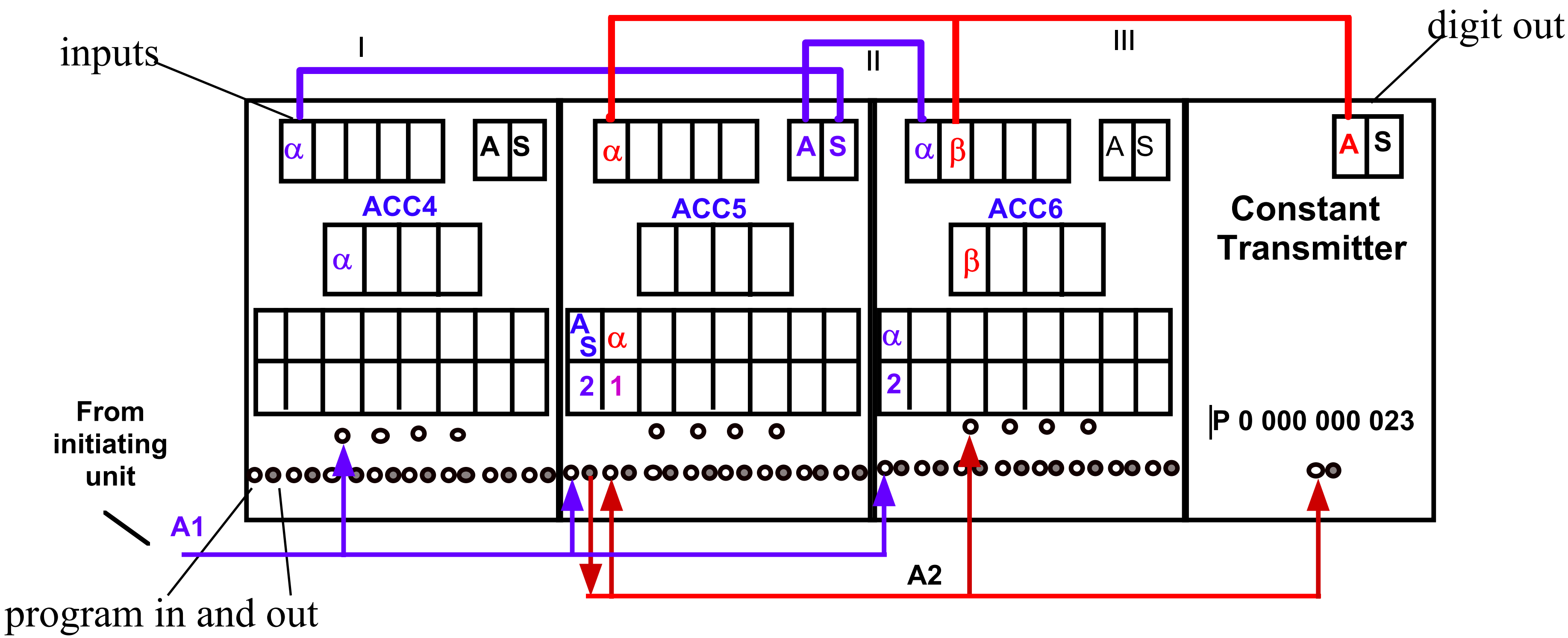
Programming ....



Programming ENIAC - an example

- Initially:
  - Accumulator 4: stores number ***a***
  - Accumulator 5: stores ***b***
  - Accumulator 6: stores ***c***
- Constant transmitter stores number 23
- After programming:
  - Accumulator 4: stores number ***a-b***
  - Accumulator 5: stores ***b+23***
  - Accumulator 6: stores ***c+2b+23***

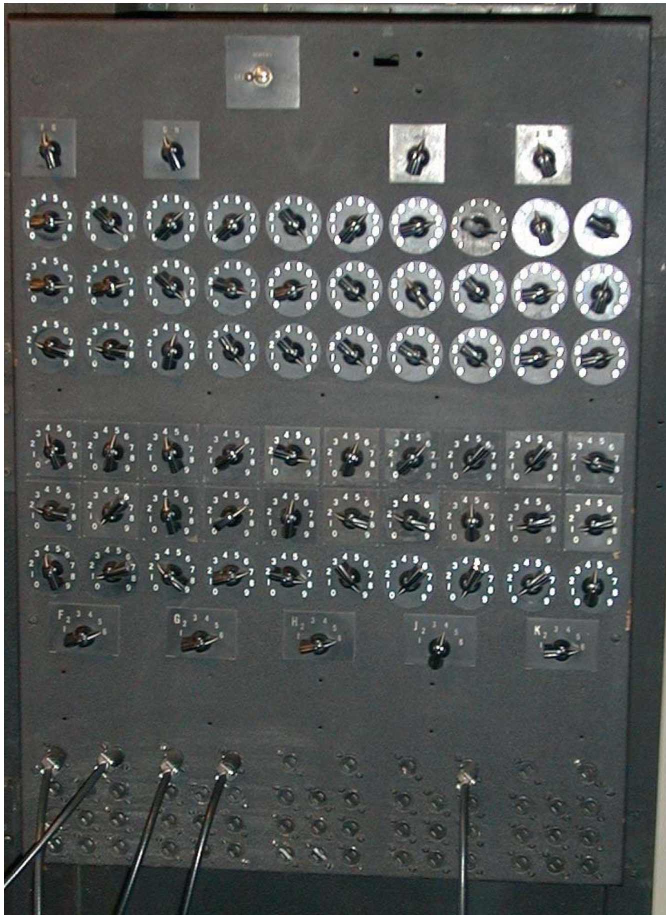
Programming ENIAC - an example



Cycles	a	b	c	-
2	*(a-b)*	*transmits 2b & -b*	*(c+2b)*	-
1	-	*(b+23)*	*(c+2b+23)*	*transmits 23*

Masterful Programming

- The **Master Programmer** allowed more complex operations:
  - Looping
  - Nested loops
  - Conditional branching
- Consists of pulse counters which emit a program pulse every time it receives an input pulse



Conditional branching

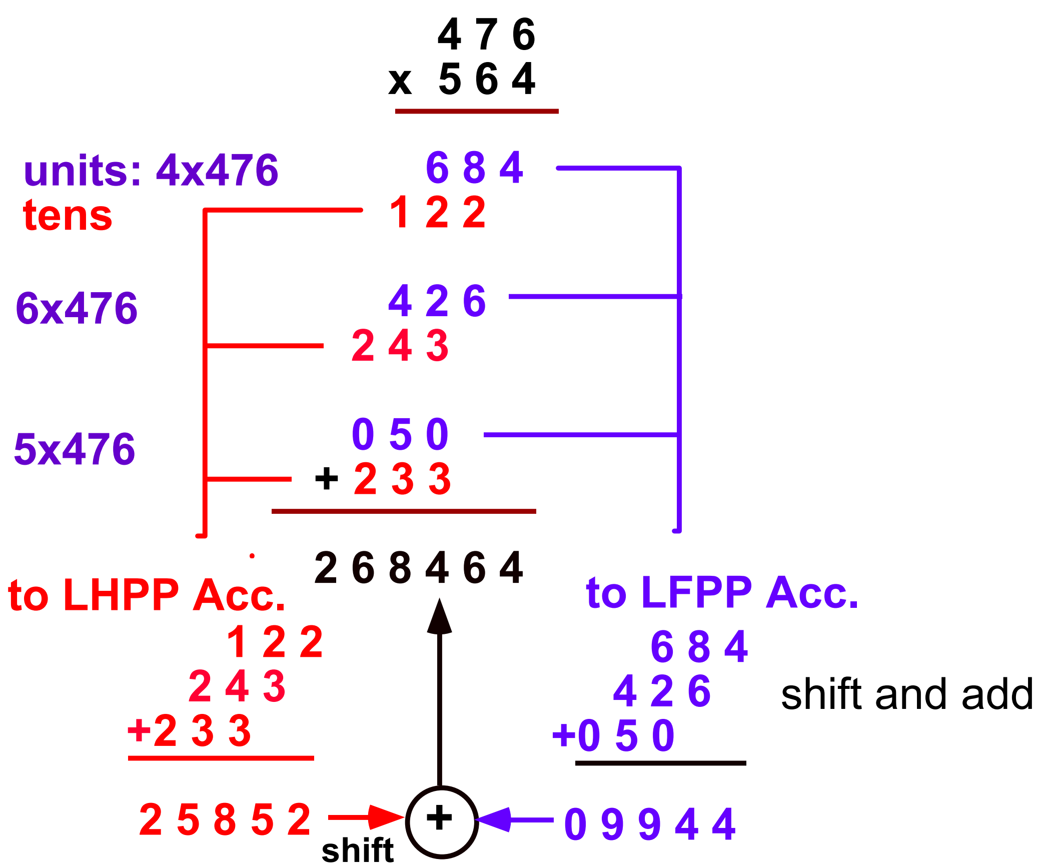
- No special hardware for ***"If...then...else"*** statement
- Involved several units

High Speed Multiplier

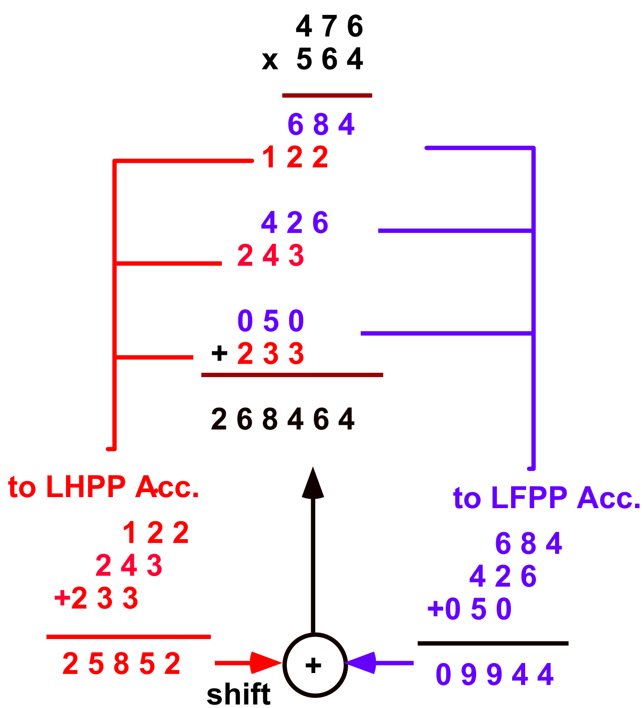
- Multiplication of a signed 10-digit with a signed *p*-digit number: *p+4* addition cycles
- How? Used multiplication tables.

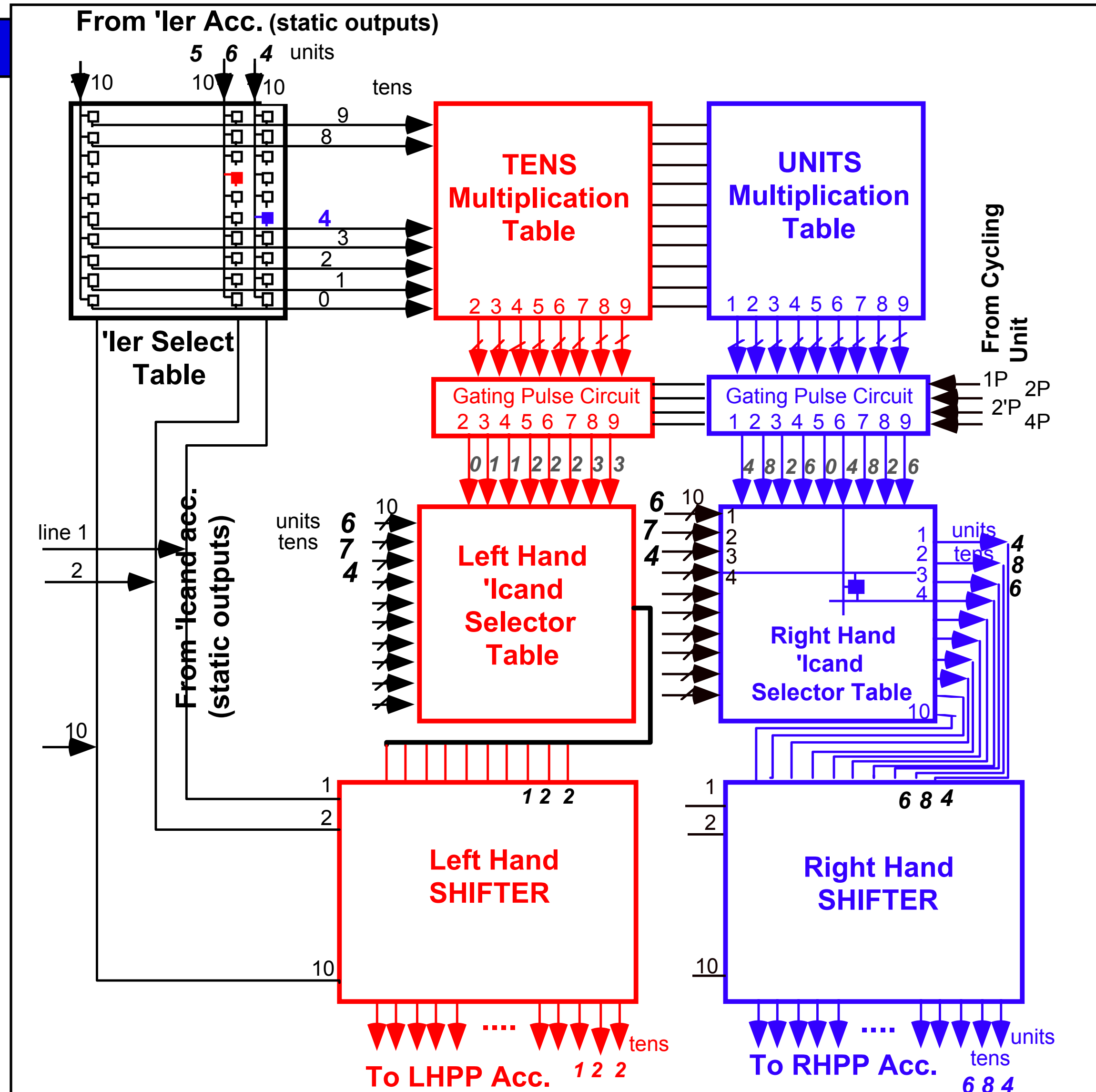
Allowed the entire multiplicand to be multiplied by consecutive digits of the multiplier

Multiplying on Eniac



Multiplier Block Diagram





Other units

- Constant transmitter
- Divider/square rooter
- Reader and printer
- Portable Function tables and panels

Chip Implementation

Vacuum tubes and transistors

ENIAC-on-a-Chip

- **Why recreating ENIAC?**
  - Historical interest
  - As tribute to ENIAC: 50th anniversary
  - Educational
- **Interesting journey into history:**
  - Reading original reports and blueprints
  - Going through archives of UPenn, Smithsonian
  - Understanding and building vacuum tube circuits

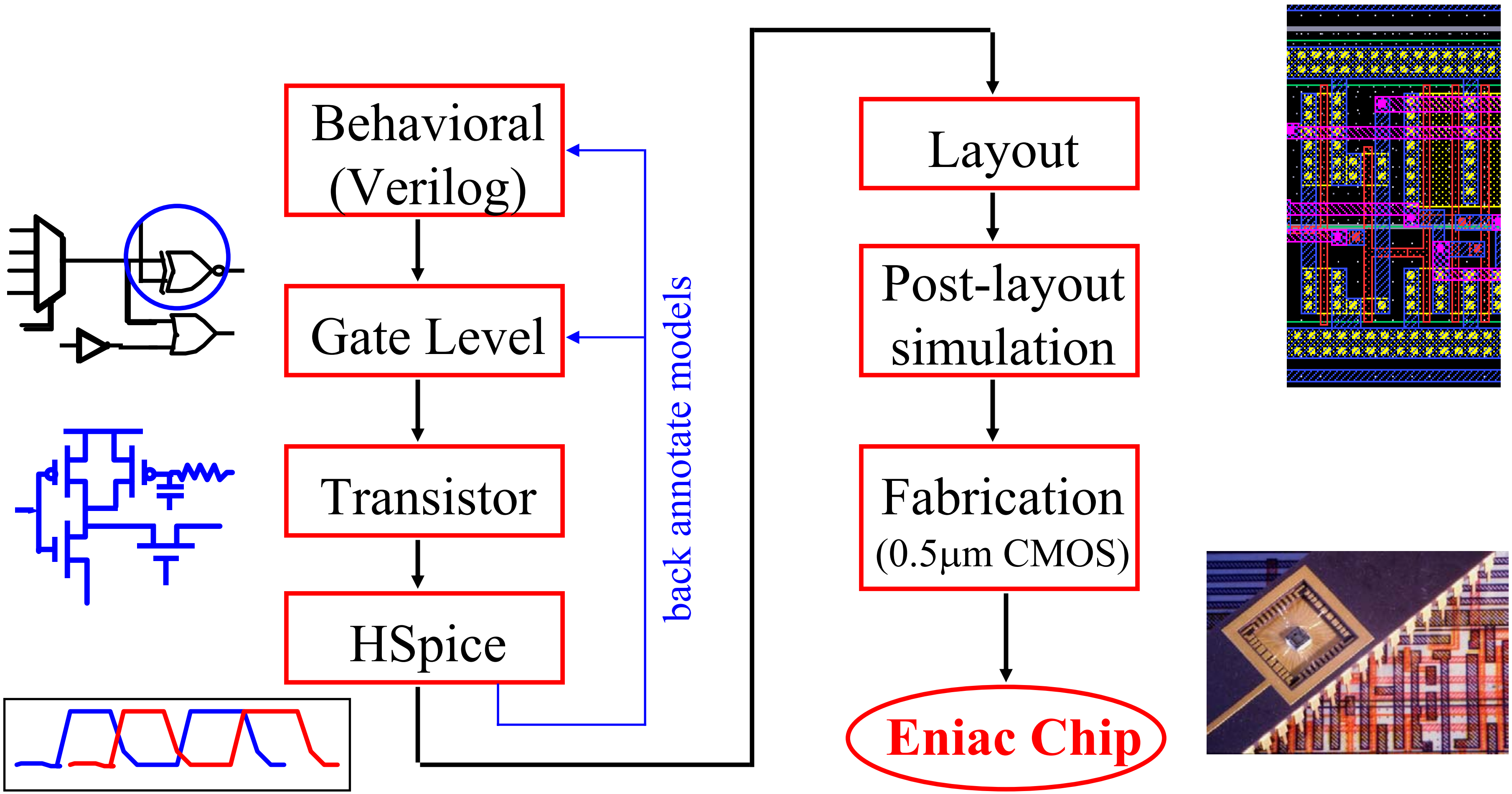
ENIAC-on-a-Chip Project Guidelines

- **Preserve the original architecture and circuits as much as possible**
- Each functional/structural unit of ENIAC has a counterpart on the chip
- Some circuit implementations on chip may be different
- Required understanding of Eniac at the circuit level

Design Approach

- Top down
- Full custom
- Handcraft each cell

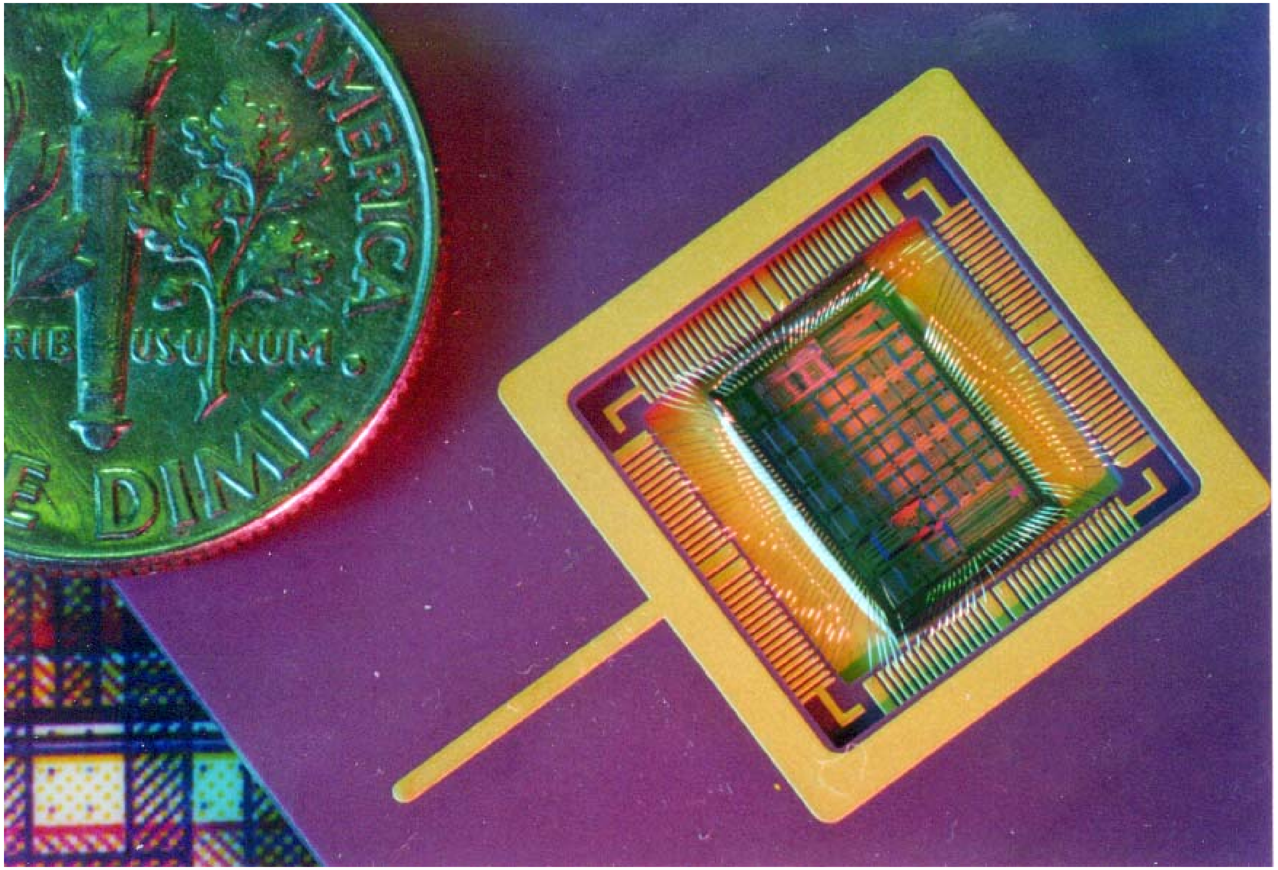
Design Flow


Behavioral
(Verilog)
Gate Level
Transistor
HSpice
back annotate models
Layout
Post-layout
simulation
Fabrication
(0.5µm CMOS)
Eniac Chip

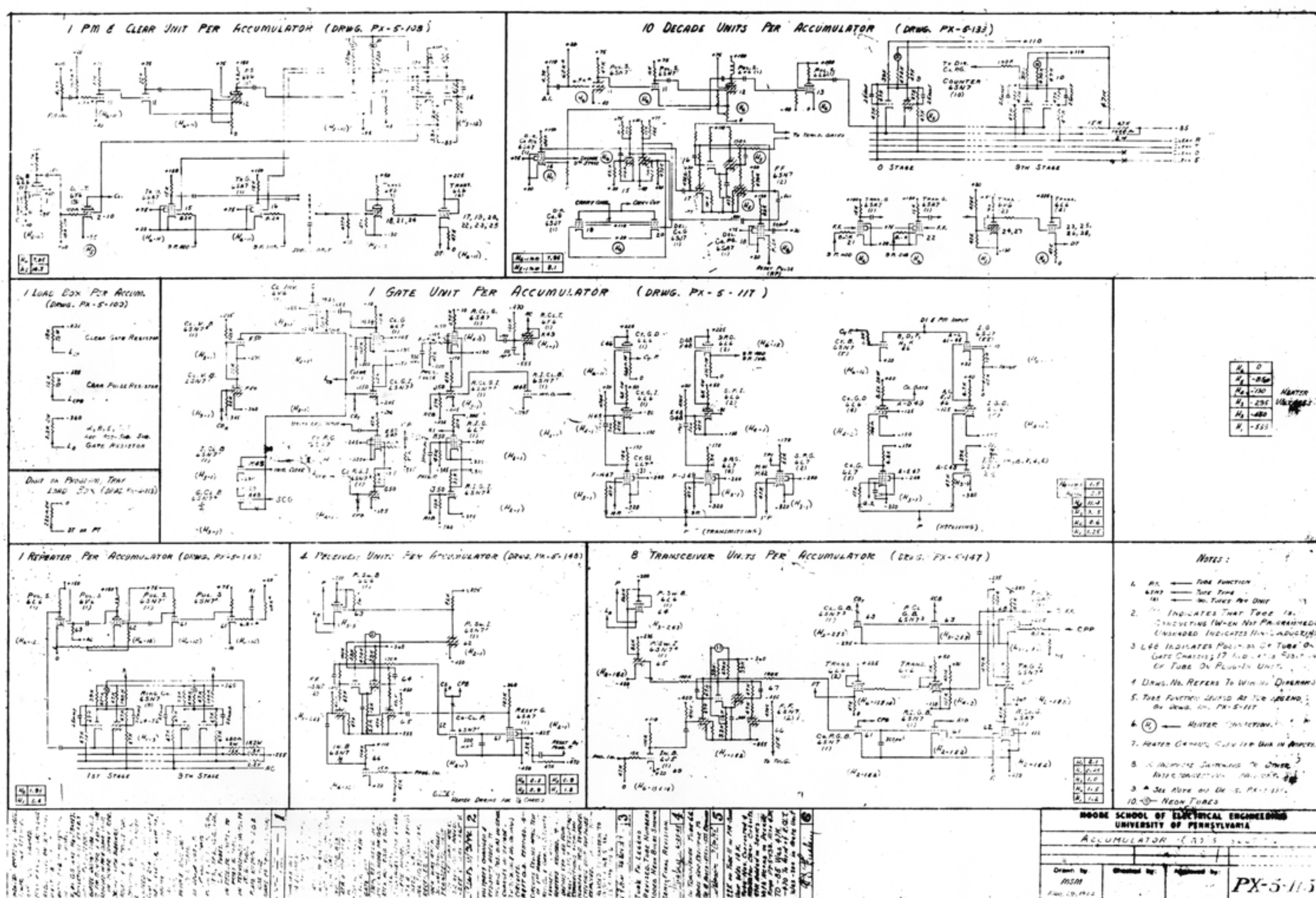
ENIAC Chip

- Fabricated in triple metal, single poly, CMOS nwell process
- 0.5 µm feature size
- Chip size: 7.44mm x 5.29 mm
- No. of transistors: 174,569
- Package: 132 pin PGA

Eniac Chip - A long journey…



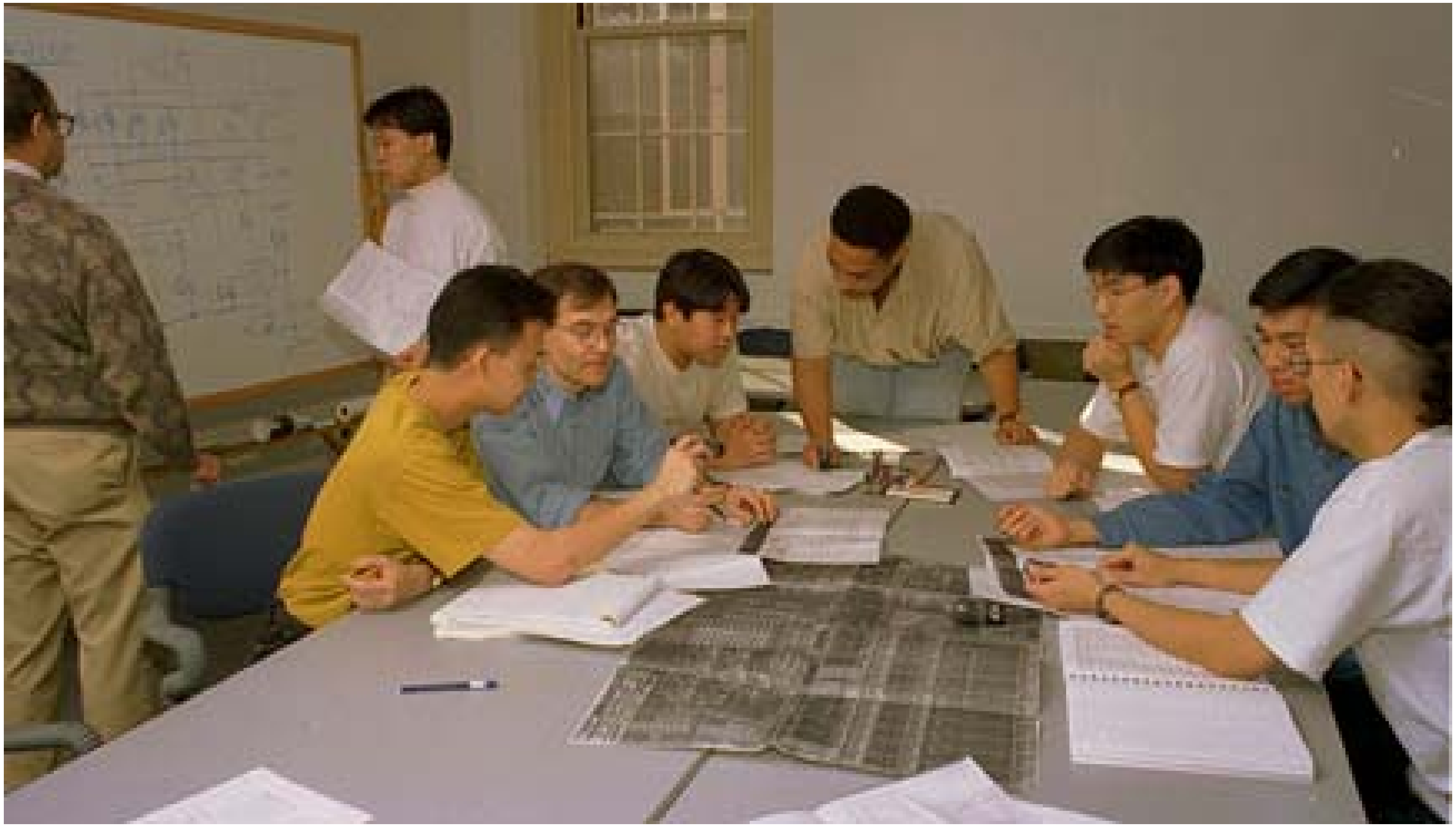
Vacuum tube circuits…



J.

(Courtesy: Univ. of Pennsylvania)

How knows vacuum tube circuits?



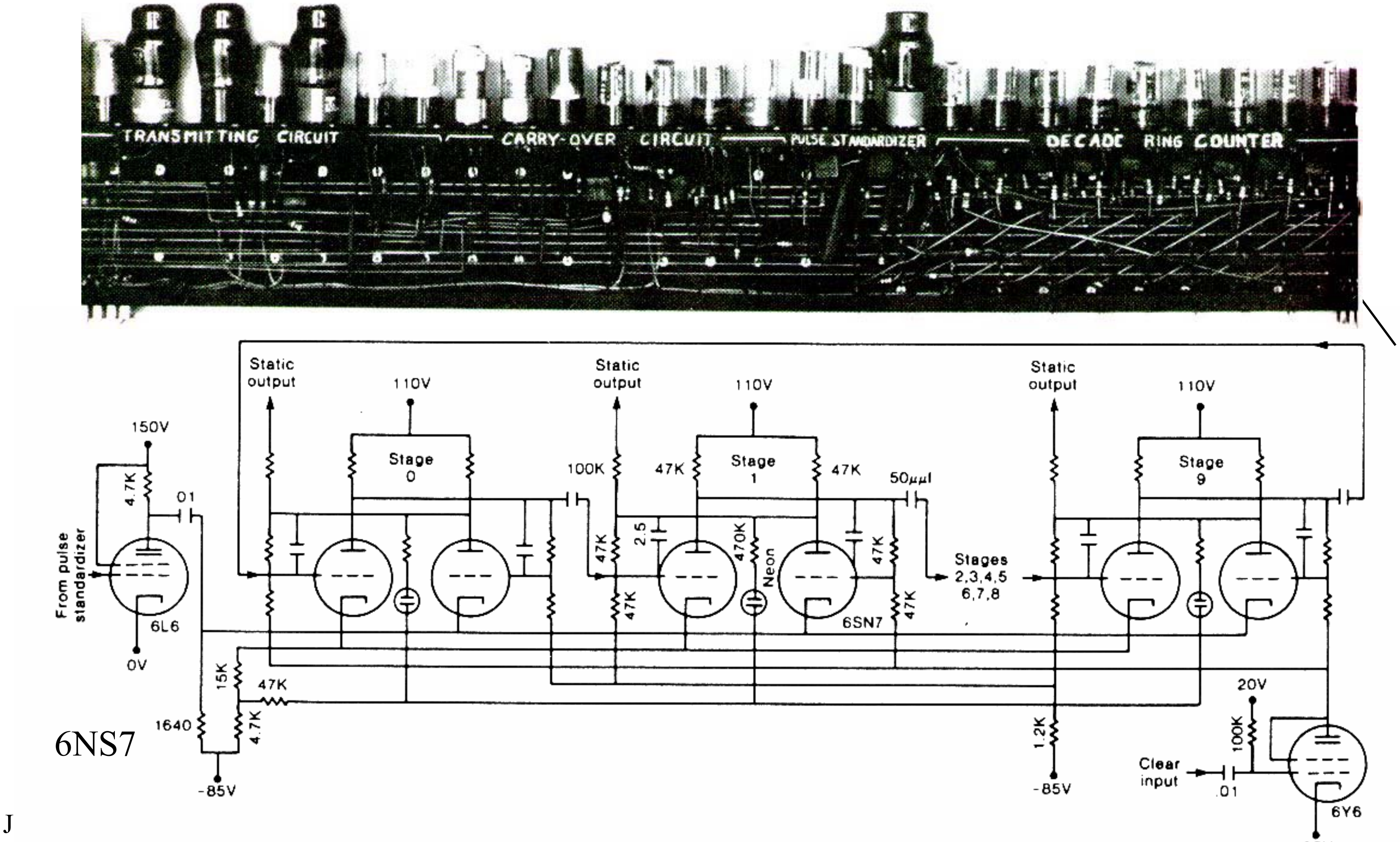
Chip Implementation - interconnection

- Data trunks: 11 lines each; up to 10 trunks
- Program trunks: 11 lines up to 10 trunks
- Static connections: Multiplier-Acc.
  2x101 connections
- Connections are main limitation on chip:
  --> Rapid reprogramming

Interconnections on Chip - rapid reprogramming

- Two digit trunks
- One programming line
- Programmable switches and shift registers

Decade Counter - vacuum tubes

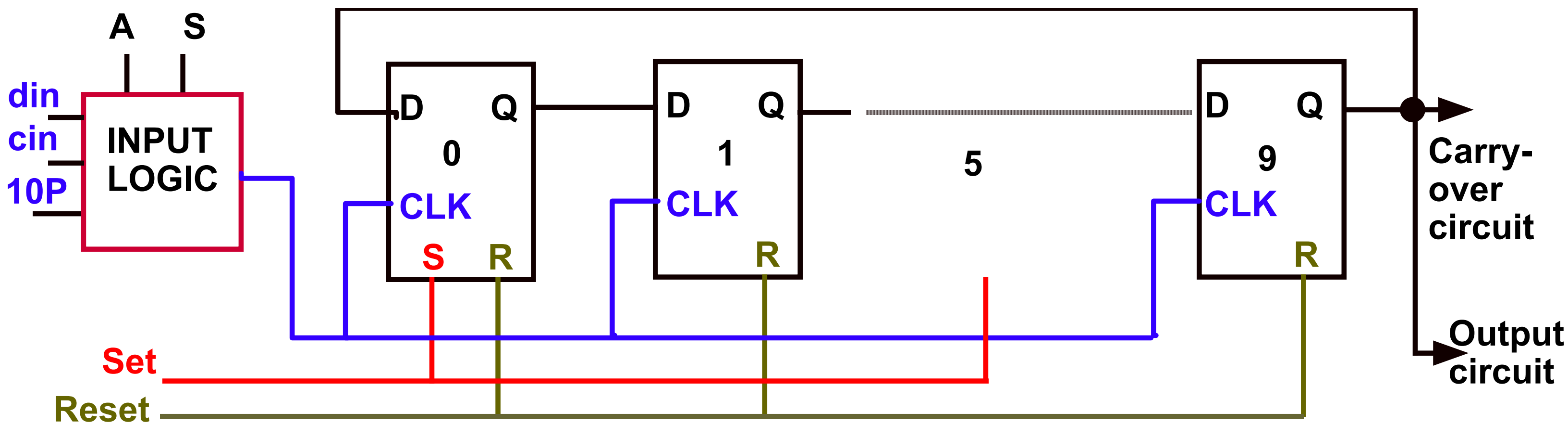


6NS7

J

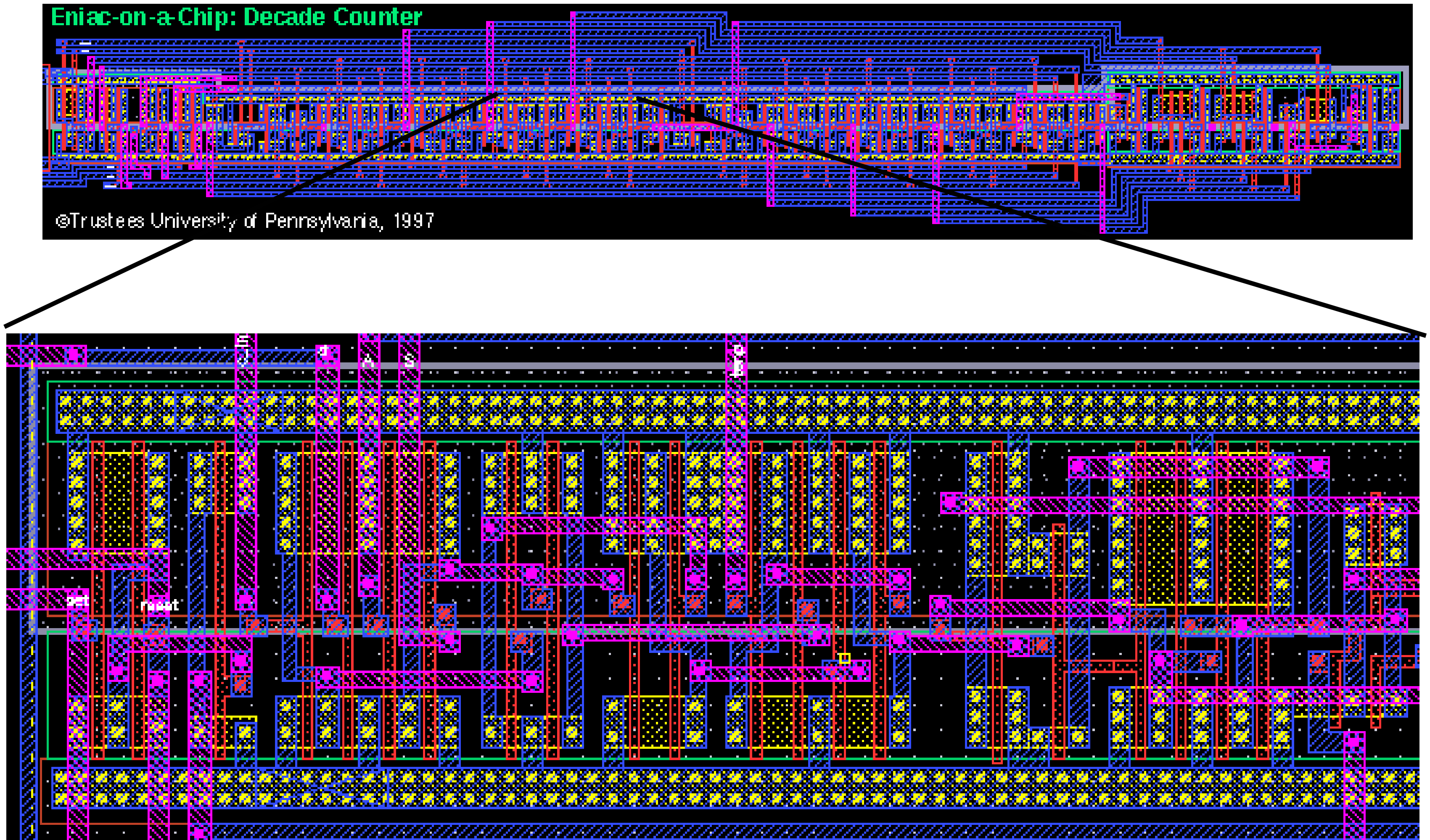
Decade counter - Shift-register

- 10-stage shift-register with d-flip-flops

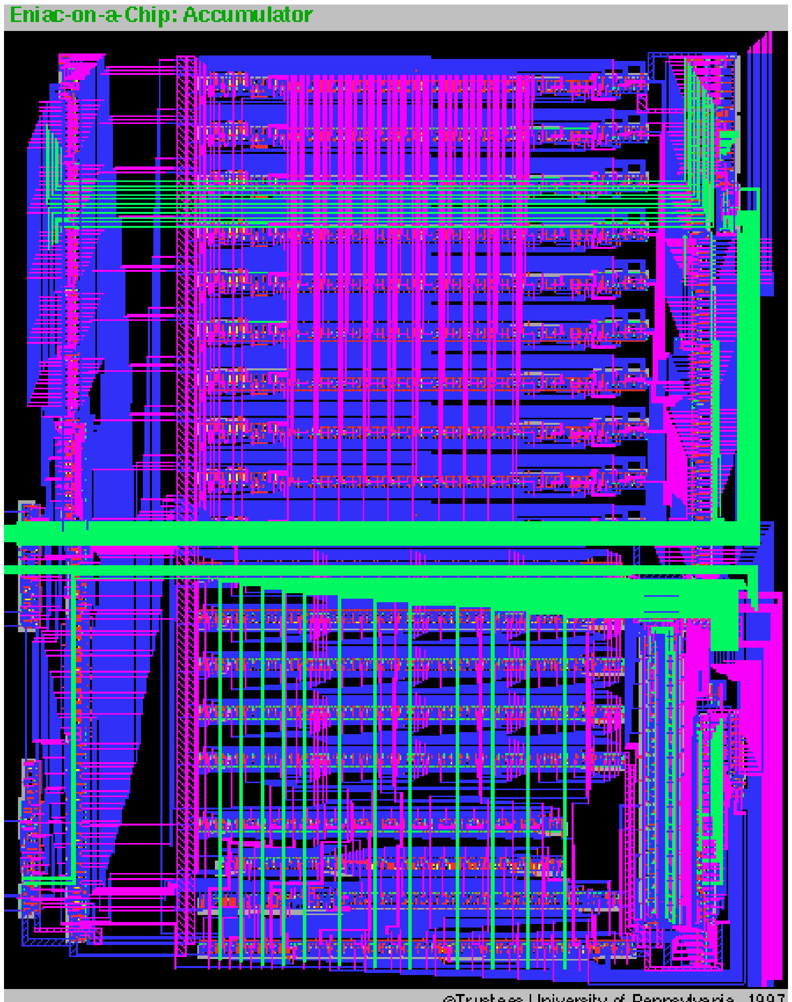


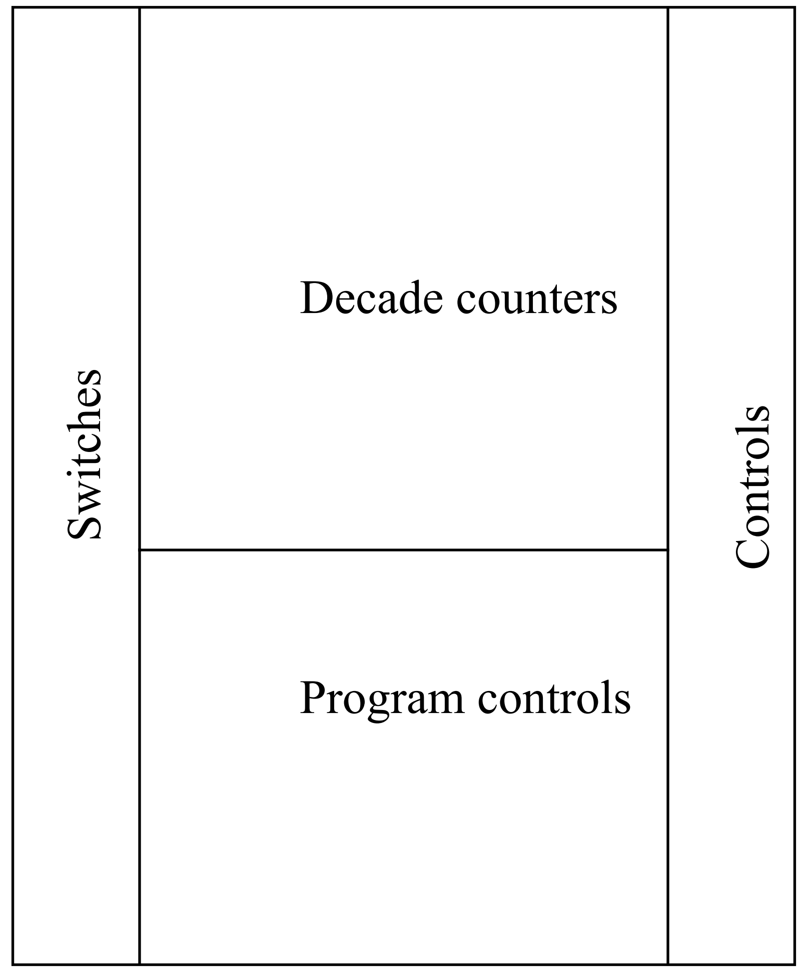
Simplified diagram

Decade counter layout

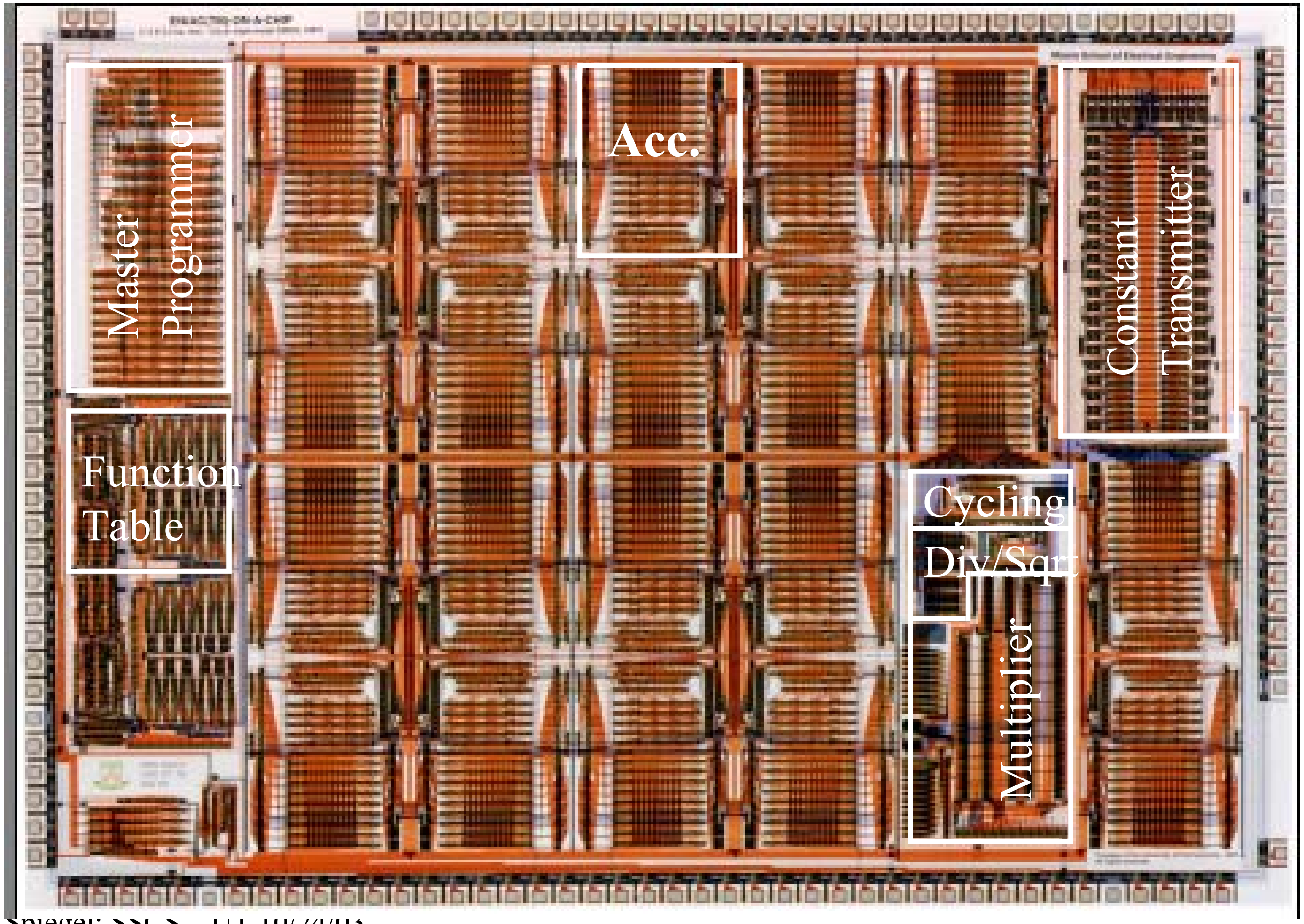


Accumulator Layout





Eniac Chip


Master Programmer
Acc.
Constant Transmitter
Function Table
Cycling
Div/Sqrt
Multiplier

Summary

- Reconstructing ENIAC was a humbling journey into the history of computing
- ENIAC was developed with emphasis on:
  - speed of operation
  - timeliness, rather than cost ($486,000 in ‘45)
  - research was replaced in favor of speedy development
  - developed for highly repetitive tasks: set-up time was not a big issue

Summary

- ENIAC's architecture:
  - dataflow
  - highly parallel
  - operations: +, -, /, x, sqrt, store, load, print, read
  - looping, nested loops and conditional branching
- ENIAC convinced scientific and industrial community that large scale, electronic computing was feasible: started the computing age.

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Eniac-on-a Chip team