

CONTENTS

Chapter 1

DESIGN CONCEPTS 1

- 1.1 Digital Hardware 2
 - 1.1.1 Standard Chips 4
 - 1.1.2 Programmable Logic Devices 4
 - 1.1.3 Custom-Designed Chips 5
- 1.2 The Design Process 6
- 1.3 Design of Digital Hardware 8
 - 1.3.1 Basic Design Loop 8
 - 1.3.2 Structure of a Computer 9
 - 1.3.3 Design of a Digital Hardware Unit 12
- 1.4 Logic Circuit Design in This Book 16
- 1.5 Theory and Practice 16
- 1.6 Binary Numbers 17
 - 1.6.1 Conversion between Decimal and Binary Systems 18
- References 20

Chapter 2

INTRODUCTION TO LOGIC CIRCUITS 21

- 2.1 Variables and Functions 22
- 2.2 Inversion 25
- 2.3 Truth Tables 26
- 2.4 Logic Gates and Networks 27
 - 2.4.1 Analysis of a Logic Network 29
- 2.5 Boolean Algebra 31
 - 2.5.1 The Venn Diagram 35
 - 2.5.2 Notation and Terminology 37
 - 2.5.3 Precedence of Operations 39
- 2.6 Synthesis Using AND, OR, and NOT Gates 39
 - 2.6.1 Sum-of-Products and Product-of-Sums Forms 41
- 2.7 NAND and NOR Logic Networks 47
- 2.8 Design Examples 52
 - 2.8.1 Three-Way Light Control 52
 - 2.8.2 Multiplexer Circuit 53
- 2.9 Introduction to CAD Tools 56

- 2.9.1 Design Entry 56
- 2.9.2 Synthesis 58
- 2.9.3 Functional Simulation 59
- 2.9.4 Physical Design 59
- 2.9.5 Timing Simulation 59
- 2.9.6 Chip Configuration 60

- 2.10 Introduction to VHDL 60
 - 2.10.1 Representation of Digital Signals in VHDL 62
 - 2.10.2 Writing Simple VHDL Code 62
 - 2.10.3 How *Not* to Write VHDL Code 64
- 2.11 Concluding Remarks 65
- 2.12 Examples of Solved Problems 66
 - Problems 69
 - References 74

Chapter 3

IMPLEMENTATION TECHNOLOGY 77

- 3.1 Transistor Switches 79
- 3.2 NMOS Logic Gates 82
- 3.3 CMOS Logic Gates 85
 - 3.3.1 Speed of Logic Gate Circuits 91
- 3.4 Negative Logic System 91
- 3.5 Standard Chips 95
 - 3.5.1 7400-Series Standard Chips 95
- 3.6 Programmable Logic Devices 98
 - 3.6.1 Programmable Logic Array (PLA) 98
 - 3.6.2 Programmable Array Logic (PAL) 101
 - 3.6.3 Programming of PLAs and PALs 103
 - 3.6.4 Complex Programmable Logic Devices (CPLDs) 105
 - 3.6.5 Field-Programmable Gate Arrays 109
 - 3.6.6 Using CAD Tools to Implement Circuits in CPLDs and FPGAs 114
 - 3.6.7 Applications of CPLDs and FPGAs 114
- 3.7 Custom Chips, Standard Cells, and Gate Arrays 114
- 3.8 Practical Aspects 118
 - 3.8.1 MOSFET Fabrication and Behavior 118
 - 3.8.2 MOSFET On-Resistance 121

- 3.8.3 Voltage Levels in Logic Gates 122
- 3.8.4 Noise Margin 123
- 3.8.5 Dynamic Operation of Logic Gates 125
- 3.8.6 Power Dissipation in Logic Gates 128
- 3.8.7 Passing 1s and 0s Through Transistor Switches 130
- 3.8.8 Fan-in and Fan-out in Logic Gates 132
- 3.9 Transmission Gates 138
 - 3.9.1 Exclusive-OR Gates 139
 - 3.9.2 Multiplexer Circuit 140
- 3.10 Implementation Details for SPLDs, CPLDs, and FPGAs 140
 - 3.10.1 Implementation in FPGAs 146
- 3.11 Concluding Remarks 149
- 3.12 Examples of Solved Problems 149
 - Problems 157
 - References 166

Chapter 4

OPTIMIZED IMPLEMENTATION OF LOGIC FUNCTIONS 167

- 4.1 Karnaugh Map 168
- 4.2 Strategy for Minimization 176
 - 4.2.1 Terminology 177
 - 4.2.2 Minimization Procedure 179
- 4.3 Minimization of Product-of-Sums Forms 182
- 4.4 Incompletely Specified Functions 184
- 4.5 Multiple-Output Circuits 186
- 4.6 Multilevel Synthesis 189
 - 4.6.1 Factoring 190
 - 4.6.2 Functional Decomposition 194
 - 4.6.3 Multilevel NAND and NOR Circuits 199
- 4.7 Analysis of Multilevel Circuits 200
- 4.8 Cubical Representation 207
 - 4.8.1 Cubes and Hypercubes 207
- 4.9 A Tabular Method for Minimization 211
 - 4.9.1 Generation of Prime Implicants 212
 - 4.9.2 Determination of a Minimum Cover 213
 - 4.9.3 Summary of the Tabular Method 219
- 4.10 A Cubical Technique for Minimization 220
 - 4.10.1 Determination of Essential Prime Implicants 222
 - 4.10.2 Complete Procedure for Finding a Minimal Cover 224
- 4.11 Practical Considerations 227
- 4.12 Examples of Circuits Synthesized from VHDL Code 228
- 4.13 Concluding Remarks 232
- 4.14 Examples of Solved Problems 233
 - Problems 241
 - References 246

Chapter 5

NUMBER REPRESENTATION AND ARITHMETIC CIRCUITS 249

- 5.1 Number Representations in Digital Systems 250
 - 5.1.1 Unsigned Integers 250
 - 5.1.2 Octal and Hexadecimal Representations 250
- 5.2 Addition of Unsigned Numbers 252
 - 5.2.1 Decomposed Full-Adder 256
 - 5.2.2 Ripple-Carry Adder 256
 - 5.2.3 Design Example 258
- 5.3 Signed Numbers 258
 - 5.3.1 Negative Numbers 258
 - 5.3.2 Addition and Subtraction 262
 - 5.3.3 Adder and Subtractor Unit 266
 - 5.3.4 Radix-Complement Schemes 267
 - 5.3.5 Arithmetic Overflow 271
 - 5.3.6 Performance Issues 272
- 5.4 Fast Adders 273
 - 5.4.1 Carry-Lookahead Adder 273
- 5.5 Design of Arithmetic Circuits Using CAD Tools 280
 - 5.5.1 Design of Arithmetic Circuits Using Schematic Capture 280
 - 5.5.2 Design of Arithmetic Circuits Using VHDL 283
 - 5.5.3 Representation of Numbers in VHDL Code 286
 - 5.5.4 Arithmetic Assignment Statements 287
- 5.6 Multiplication 291
 - 5.6.1 Array Multiplier for Unsigned Numbers 293
 - 5.6.2 Multiplication of Signed Numbers 293
- 5.7 Other Number Representations 295
 - 5.7.1 Fixed-Point Numbers 295
 - 5.7.2 Floating-Point Numbers 297

- 5.7.3 Binary-Coded-Decimal Representation 299
- 5.8 ASCII Character Code 302
- 5.9 Examples of Solved Problems 305
 - Problems 312
 - References 316

Chapter 6

COMBINATIONAL-CIRCUIT BUILDING BLOCKS 317

- 6.1 Multiplexers 318
 - 6.1.1 Synthesis of Logic Functions Using Multiplexers 323
 - 6.1.2 Multiplexer Synthesis Using Shannon's Expansion 326
- 6.2 Decoders 331
 - 6.2.1 Demultiplexers 335
- 6.3 Encoders 337
 - 6.3.1 Binary Encoders 337
 - 6.3.2 Priority Encoders 338
- 6.4 Code Converters 339
- 6.5 Arithmetic Comparison Circuits 340
- 6.6 VHDL for Combinational Circuits 341
 - 6.6.1 Assignment Statements 341
 - 6.6.2 Selected Signal Assignment 342
 - 6.6.3 Conditional Signal Assignment 346
 - 6.6.4 Generate Statements 350
 - 6.6.5 Concurrent and Sequential Assignment Statements 352
 - 6.6.6 Process Statement 352
 - 6.6.7 Case Statement 358
 - 6.6.8 VHDL Operators 361
- 6.7 Concluding Remarks 365
- 6.8 Examples of Solved Problems 365
 - Problems 374
 - References 379

Chapter 7

FLIP-FLOPS, REGISTERS, COUNTERS, AND A SIMPLE PROCESSOR 381

- 7.1 Basic Latch 383
- 7.2 Gated SR Latch 385
 - 7.2.1 Gated SR Latch with NAND Gates 387
- 7.3 Gated D Latch 388
 - 7.3.1 Effects of Propagation Delays 390
- 7.4 Master-Slave and Edge-Triggered D Flip-Flops 391
 - 7.4.1 Master-Slave D Flip-Flop 391
 - 7.4.2 Edge-Triggered D Flip-Flop 391
 - 7.4.3 D Flip-Flops with Clear and Preset 395
 - 7.4.4 Flip-Flop Timing Parameters 396
- 7.5 T Flip-Flop 398
 - 7.5.1 Configurable Flip-Flops 399
- 7.6 JK Flip-Flop 400
- 7.7 Summary of Terminology 401
- 7.8 Registers 401
 - 7.8.1 Shift Register 401
 - 7.8.2 Parallel-Access Shift Register 402
- 7.9 Counters 404
 - 7.9.1 Asynchronous Counters 404
 - 7.9.2 Synchronous Counters 406
 - 7.9.3 Counters with Parallel Load 411
- 7.10 Reset Synchronization 411
- 7.11 Other Types of Counters 415
 - 7.11.1 BCD Counter 415
 - 7.11.2 Ring Counter 416
 - 7.11.3 Johnson Counter 417
 - 7.11.4 Remarks on Counter Design 418
- 7.12 Using Storage Elements with CAD Tools 418
 - 7.12.1 Including Storage Elements in Schematics 418
 - 7.12.2 Using VHDL Constructs for Storage Elements 421
- 7.13 Using Registers and Counters with CAD Tools 426
 - 7.13.1 Including Registers and Counters in Schematics 426
 - 7.13.2 Registers and Counters in VHDL Code 428
 - 7.13.3 Using VHDL Sequential Statements for Registers and Counters 430
- 7.14 Design Examples 438
 - 7.14.1 Bus Structure 438
 - 7.14.2 Simple Processor 450
 - 7.14.3 Reaction Timer 463
 - 7.14.4 Register Transfer Level (RTL) Code 468
- 7.15 Timing Analysis of Flip-Flop Circuits 469
- 7.16 Concluding Remarks 471
- 7.17 Examples of Solved Problems 472
 - Problems 476
 - References 483

Chapter 8**SYNCHRONOUS SEQUENTIAL
CIRCUITS 485**

- 8.1 Basic Design Steps 487
 - 8.1.1 State Diagram 487
 - 8.1.2 State Table 489
 - 8.1.3 State Assignment 489
 - 8.1.4 Choice of Flip-Flops and Derivation of Next-State and Output Expressions 491
 - 8.1.5 Timing Diagram 492
 - 8.1.6 Summary of Design Steps 494
- 8.2 State-Assignment Problem 497
 - 8.2.1 One-Hot Encoding 500
- 8.3 Mealy State Model 502
- 8.4 Design of Finite State Machines Using CAD Tools 507
 - 8.4.1 VHDL Code for Moore-Type FSMs 508
 - 8.4.2 Synthesis of VHDL Code 510
 - 8.4.3 Simulating and Testing the Circuit 512
 - 8.4.4 An Alternative Style of VHDL Code 513
 - 8.4.5 Summary of Design Steps When Using CAD Tools 513
 - 8.4.6 Specifying the State Assignment in VHDL Code 515
 - 8.4.7 Specification of Mealy FSMs Using VHDL 517
- 8.5 Serial Adder Example 519
 - 8.5.1 Mealy-Type FSM for Serial Adder 520
 - 8.5.2 Moore-Type FSM for Serial Adder 522
 - 8.5.3 VHDL Code for the Serial Adder 524
- 8.6 State Minimization 528
 - 8.6.1 Partitioning Minimization Procedure 530
 - 8.6.2 Incompletely Specified FSMs 537
- 8.7 Design of a Counter Using the Sequential Circuit Approach 539
 - 8.7.1 State Diagram and State Table for a Modulo-8 Counter 539
 - 8.7.2 State Assignment 539
 - 8.7.3 Implementation Using D-Type Flip-Flops 541
 - 8.7.4 Implementation Using JK-Type Flip-Flops 542
 - 8.7.5 Example—A Different Counter 547
- 8.8 FSM as an Arbiter Circuit 549
 - 8.8.1 Implementation of the Arbiter Circuit 553

- 8.8.2 Minimizing the Output Delays for an FSM 556

- 8.8.3 Summary 557

- 8.9 Analysis of Synchronous Sequential Circuits 557
- 8.10 Algorithmic State Machine (ASM) Charts 561
- 8.11 Formal Model for Sequential Circuits 565
- 8.12 Concluding Remarks 566
- 8.13 Examples of Solved Problems 567
 - Problems 576
 - References 581

Chapter 9**ASYNCHRONOUS SEQUENTIAL
CIRCUITS 583**

- 9.1 Asynchronous Behavior 584
- 9.2 Analysis of Asynchronous Circuits 588
- 9.3 Synthesis of Asynchronous Circuits 596
- 9.4 State Reduction 609
- 9.5 State Assignment 624
 - 9.5.1 Transition Diagram 627
 - 9.5.2 Exploiting Unspecified Next-State Entries 630
 - 9.5.3 State Assignment Using Additional State Variables 634
 - 9.5.4 One-Hot State Assignment 639
- 9.6 Hazards 640
 - 9.6.1 Static Hazards 641
 - 9.6.2 Dynamic Hazards 645
 - 9.6.3 Significance of Hazards 646
- 9.7 A Complete Design Example 648
 - 9.7.1 The Vending-Machine Controller 648
- 9.8 Concluding Remarks 653
- 9.9 Examples of Solved Problems 655
 - Problems 663
 - References 667

Chapter 10**DIGITAL SYSTEM DESIGN 669**

- 10.1 Building Block Circuits 670
 - 10.1.1 Flip-Flops and Registers with Enable Inputs 670

- 10.1.2 Shift Registers with Enable Inputs 672
- 10.1.3 Static Random Access Memory (SRAM) 674
- 10.1.4 SRAM Blocks in PLDs 679
- 10.2 Design Examples 679
 - 10.2.1 A Bit-Counting Circuit 679
 - 10.2.2 ASM Chart Implied Timing Information 681
 - 10.2.3 Shift-and-Add Multiplier 683
 - 10.2.4 Divider 692
 - 10.2.5 Arithmetic Mean 702
 - 10.2.6 Sort Operation 708
- 10.3 Clock Synchronization 719
 - 10.3.1 Clock Skew 719
 - 10.3.2 Flip-Flop Timing Parameters 720
 - 10.3.3 Asynchronous Inputs to Flip-Flops 723
 - 10.3.4 Switch Debouncing 724
- 10.4 Concluding Remarks 724
 - Problems 726
 - References 730

Chapter 11

TESTING OF LOGIC CIRCUITS 731

- 11.1 Fault Model 732
 - 11.1.1 Stuck-at Model 732
 - 11.1.2 Single and Multiple Faults 733
 - 11.1.3 CMOS Circuits 733
- 11.2 Complexity of a Test Set 733
- 11.3 Path Sensitizing 735
 - 11.3.1 Detection of a Specific Fault 737
- 11.4 Circuits with Tree Structure 739
- 11.5 Random Tests 740
- 11.6 Testing of Sequential Circuits 743
 - 11.6.1 Design for Testability 743
- 11.7 Built-in Self-Test 747
 - 11.7.1 Built-in Logic Block Observer 751
 - 11.7.2 Signature Analysis 753
 - 11.7.3 Boundary Scan 754
- 11.8 Printed Circuit Boards 754
 - 11.8.1 Testing of PCBs 756
 - 11.8.2 Instrumentation 757
- 11.9 Concluding Remarks 758
 - Problems 758
 - References 761

Chapter 12

COMPUTER AIDED DESIGN TOOLS 763

- 12.1 Synthesis 764
 - 12.1.1 Netlist Generation 764
 - 12.1.2 Gate Optimization 764
 - 12.1.3 Technology Mapping 766
- 12.2 Physical Design 770
 - 12.2.1 Placement 773
 - 12.2.2 Routing 774
 - 12.2.3 Static Timing Analysis 775
- 12.3 Concluding Remarks 777
 - References 777

Appendix A

VHDL REFERENCE 779

- A.1 Documentation in VHDL Code 780
- A.2 Data Objects 780
 - A.2.1 Data Object Names 780
 - A.2.2 Data Object Values and Numbers 780
 - A.2.3 SIGNAL Data Objects 781
 - A.2.4 BIT and BIT_VECTOR Types 781
 - A.2.5 STD_LOGIC and STD_LOGIC_VECTOR Types 782
 - A.2.6 STD_ULOGIC Type 782
 - A.2.7 SIGNED and UNSIGNED Types 783
 - A.2.8 INTEGER Type 784
 - A.2.9 BOOLEAN Type 784
 - A.2.10 ENUMERATION Type 784
 - A.2.11 CONSTANT Data Objects 785
 - A.2.12 VARIABLE Data Objects 785
 - A.2.13 Type Conversion 785
 - A.2.14 Arrays 786
- A.3 Operators 787
- A.4 VHDL Design Entity 787
 - A.4.1 ENTITY Declaration 788
 - A.4.2 Architecture 788
- A.5 Package 790
- A.6 Using Subcircuits 791
 - A.6.1 Declaring a COMPONENT in a Package 793
- A.7 Concurrent Assignment Statements 794
 - A.7.1 Simple Signal Assignment 795
 - A.7.2 Assigning Signal Values Using OTHERS 796

- A.7.3 Selected Signal Assignment 797
- A.7.4 Conditional Signal Assignment 798
- A.7.5 GENERATE Statement 799
- A.8 Defining an Entity with GENERICS 799
- A.9 Sequential Assignment Statements 800
 - A.9.1 PROCESS Statement 800
 - A.9.2 IF Statement 802
 - A.9.3 CASE Statement 802
 - A.9.4 Loop Statements 803
 - A.9.5 Using a Process for a Combinational Circuit 803
 - A.9.6 Statement Ordering 805
 - A.9.7 Using a VARIABLE in a PROCESS 806
- A.10 Sequential Circuits 811
 - A.10.1 A Gated D Latch 811
 - A.10.2 D Flip-Flop 812
 - A.10.3 Using a WAIT UNTIL Statement 813
 - A.10.4 A Flip-Flop with Asynchronous Reset 814
 - A.10.5 Synchronous Reset 814
 - A.10.6 Registers 814
 - A.10.7 Shift Registers 817
 - A.10.8 Counters 819
 - A.10.9 Using Subcircuits with GENERIC Parameters 819
 - A.10.10 A Moore-Type Finite State Machine 822
 - A.10.11 A Mealy-Type Finite State Machine 824
- A.11 Common Errors in VHDL Code 827
- A.12 Concluding Remarks 830
 - References 831

Appendix B

TUTORIAL 1—INTRODUCTION TO QUARTUS II CAD SOFTWARE 833

- B.1 Introduction 833
 - B.1.1 Getting Started 834
- B.2 Starting a New Project 836
- B.3 Design Entry Using Schematic Capture 838
 - B.3.1 Using the Block Editor 838
 - B.3.2 Synthesizing a Circuit from the Schematic 846
 - B.3.3 Simulating the Designed Circuit 848
- B.4 Design Entry Using VHDL 854
 - B.4.1 Create Another Project 854
 - B.4.2 Using the Text Editor 854
 - B.4.3 Synthesizing a Circuit from the VHDL Code 856
 - B.4.4 Performing Functional Simulation 856

- B.4.5 Using Quartus II to Debug VHDL Code 856
- B.5 Mixing Design-Entry Methods 857
 - B.5.1 Using Schematic Entry at the Top Level 857
 - B.5.2 Using VHDL at the Top Level 860
- B.6 Quartus II Windows 861
- B.7 Concluding Remarks 862

Appendix C

TUTORIAL 2—IMPLEMENTING CIRCUITS IN ALTERA DEVICES 863

- C.1 Implementing a Circuit in a Cyclone II FPGA 863
 - C.1.1 Selecting a Chip 863
 - C.1.2 Compiling the Project 864
 - C.1.3 Performing Timing Simulation 865
 - C.1.4 Using the Chip Planner 867
- C.2 Making Pin Assignments 871
 - C.2.1 Recompiling the Project with Pin Assignments 874
- C.3 Programming and Configuring the FPGA Device 874
 - C.3.1 JTAG Programming 874
- C.4 Concluding Remarks 877

Appendix D

TUTORIAL 3—USING QUARTUS II TOOLS 879

- D.1 Implementing an Adder using Quartus II 879
 - D.1.1 Simulating the Circuit 880
 - D.1.2 Timing Simulation 882
 - D.1.3 Implementing the Adder Circuit on the DE2 Board 885
- D.2 Using an LPM Module 885
- D.3 Design of a Finite State Machine 892
- D.4 Concluding Remarks 897

Appendix E
COMMERCIAL DEVICES 899

- E.1 Simple PLDs 899
 - E.1.1 The 22V10 PAL Device 899
- E.2 Complex PLDs 901
 - E.2.1 Altera MAX 7000 902
- E.3 Field-Programmable Gate Arrays 904
 - E.3.1 Altera FLEX 10K 904
 - E.3.2 Xilinx XC4000 908
 - E.3.3 Altera APEX 20K 909
 - E.3.4 Altera Stratix 910
 - E.3.5 Altera Cyclone, Cyclone II, and Cyclone III 911
 - E.3.6 Altera Stratix II and Stratix III 911
 - E.3.7 Xilinx Virtex 912
 - E.3.8 Xilinx Virtex-II and Virtex-II Pro, Virtex-4, and Virtex-5 914
 - E.3.9 Xilinx Spartan-3 914
- E.4 Transistor-Transistor Logic 914
 - E.4.1 TTL Circuit Families 915
 - References 916

ANSWERS 919**INDEX 934**